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Cost-Effective Thin n-type Silicon Solar Cells with Rear Emitter

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The silicon solar cells achieved relatively low prices in the last years and to introduce a new structure in the PV industry, the amount of silicon per watt has to be reduced, requiring a cost-effective manufacturing process. The use of n-type solar grade silicon has the advantages of presenting higher minority carrier lifetime than p-type one and the absence of the boron-oxygen defects. The aim of this paper is to present the development of 100 μm thick n^+np^+ silicon solar cells with a selective p^+ rear emitter formed by boron deposited by spin-on and an Al/Ag grid deposited by screen-printing. The firing temperature of Ag/Al (rear face) e Ag (front face) was optimized and the temperature of 840 °C produced the devices with higher efficiency. The solar cells presented efficiencies of 16%, achieving a low silicon consumption of 1.6 g/W, 40% lower than thick p-type devices produced by the same process.

Keywords*: thin Si solar cells, n-type Si, rear emitter.*

1. Introduction

Most industrial solar cells are produced by using 180 μm thick silicon wafers grown by the Czochralski (Cz) method (monocrystalline wafers) or by block-casting process (multicrystalline wafers). The n^+pp^+ structure with the front phosphorus doped emitter and the p^+ BSF (back surface field) formed by aluminum paste and diffusion in a belt furnace has been a standard in the photovoltaic (PV) industry in the last decades. Efficiencies of 17% - 19% are currently obtained[1]. The silicon wafer represents 52% of the solar cell cost and 28% of the PV module cost, as reported by the International Technology Roadmap for Photovoltaic[2]. Thinner wafers can be used to reduce the PV module cost and there is a perspective that in 2029 the industry will probably use 120 μm wafers with 120 μm kerf loss, reducing the silicon consumption by 27% if breakage will not increase and efficiency will be maintained[2,3].

The n^+pp^+ structure based on screen-printed Al layer cannot be applied to the thin wafers bearing in mind the wafer bowing[4]. The bow is produced during the thermal step performed to diffuse Al into a silicon in a belt furnace due to the different thermal coefficients of expansion of aluminum layer and silicon. The wafer bowing can lead to cracking during soldering and lamination processes to assemble the PV modules.

Although the p-type silicon is used to manufacture solar cells, it is susceptible to light-induced degradation (LID) due to boron-oxygen interaction[5-8]. The open circuit voltage of p-type devices can decrease in order of 3% - 4% in the first hours of solar radiation exposure due to the reduction of minority carrier lifetime[5]. On the other hand, the devices processed in n-type Si, doped with phosphorus, did not present such degradation. Glunz[a] et al. reported that the minority carrier lifetime reduction was also observed in p-type cells kept under reverse bias voltage[5]. Therefore, performance degradation of p-type devices is caused by the injection of excess minority carriers produced by photons or by reverse bias and the interaction of the carriers with B-O complexes[5,6].

Besides the absence of LID, the efficiency of n-type devices are less affected by metallic contaminants common in silicon solar cell production[9,10]. For instance, the interstitial Fe is more effective in capturing electrons than holes due to the positive charge state. Since electrons are the minority carriers in p-type wafers, this metallic impurity causes a lower minority carrier lifetime in p-type than n-type silicon[10].

In the last years, review papers on n-type silicon solar cells were published pointing out the advantages of these devices and the difficulties concerning the industrial production[11-14]. The structures developed in n-type silicon can be categorized as: 1) front-emitter solar cell (p^+n ou p^+nn^+) such as passivated emitter and rear cell (PERC), passivated emitter rear totally diffused (PERT), passivated emitter rear locally diffused (PERL), emitter wrap-through and metal wrap-through (MWT); 2) back junction with front surface field (FSF), with aluminum or boron doped emitter and interdigitated back contact (IBC) cells; 3) hetero-junction with intrinsic thin layer (HIT) solar cells and 4) ion implanted devices (generally with rear emitters). With the exception of HIT structure, high efficiency solar cells are produced with boron doped emitters obtained by diffusion with BBr_3 as source or by ion implantation. The former boron source remains as a standard to produce solar cells, even though the boron rich layer (BRL) formed during the thermal process can hinder surface passivation and can degrade the minority carrier lifetime[15].

The IBC and HIT are high efficiency solar cells fabricated in n-type wafers, achieving the efficiency of 25%, but high quality surface passivation and high quality wafers are needed[12,14,16].

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Efficiencies near 22% were reported for p^+nn^+ PERT solar cell[17]. In this solar cell, boron and phosphorus diffusions were carried out by using BBr_3 and $POCl_3$, oxide growth steps were implemented and SiO_2 layer passivated the rear face and Al_2O_3/SiN_x passivated the front face. An aluminum layer (2 µm thick) was deposited by e-beam evaporation on the whole rear face, contacting the rear face by holes in the SiO_2 layer. The front metal grid was deposited by electroplating of Cu/Ni/Ag. Otherwise, Lu et al.[18] presented a p^+nn^+ cell without an Al layer deposited on the rear face, achieving an efficiency of around 21%. The rear face was passivated by SiO_2 thermally grown layer and on the front face was deposited the $SiO_2/Al_2O_3/SiN_x$ stack layer. The n^+ region was obtained by ion implantation and p^+ was produced by boron diffusion with BBr_3 as source. Rear emitter solar cells were developed by using BBr_3 as a boron source and Cz and epitaxially (epi) grown n-type wafers. The efficiencies near to 22% were reached[13].

In order to substitute the BBr_3 as boron source, Rhotard et al.[19] deposited a borosilicate layer by atmospheric pressure chemical vapor deposition (APCVD) and performed a B/P co-diffusion during the thermal step. They reported a dark saturation current density of 80 fA/cm^2, allowing for an implied open circuit voltage of 650 mV. By using plasma enhanced chemical vapor technique to deposit a borosilicate layer, Wehmeier et al.[20] produced n-type PERT cells with rear junction (n^+np^+) that reached the efficiency of 20.7%. Spin-on dopants have also been used as source to form the heavily doped regions in diffusion thermal steps[21-23]. Boric acid was used as a boron dopant by Das et al.[22] to produce n-type back junction solar cells, achieving efficiencies over 20% in 4 cm^2 devices passivated with SiO_2-SiN_x stack. A comparison of n-type PERT solar cells (p^+nn^+) with boron emitter formed by spin-on coating (boric acid), screen-printing of boron paste, ion implantation, and APCVD was presented by Ryu et al.[23]. The authors showed that different B emitter technologies can produce devices with efficiencies nearly of 20%[23].

Concerning thin n-type Si wafers, the heterojunction solar cells were studied by using commercial 200 µm-thick Cz wafers thinned until to achieve the thickness of 60 µm[24]. The heterojunction was formed by the deposition of (p^+) a-Si:H and (i) a-Si:H on the front face and (i)a-Si:H and (n^+)a-Si:H on the rear face. The front and rear contacts were established with ITO (indium tin oxide) and sputtered Ag, respectively. The main conclusion reported is concerning that thin cells presented higher efficiency than thick cells when lower quality Cz silicon are used and simulations indicated the 24% efficient solar cells are achievable[24]. Although these structures can achieve high efficiencies, several processing steps are needed and the manufacturing process may be not cost-effective. Otherwise, large area PERC devices, that is, without diffusion on the rear face and both faces passivated by SiN_x:H, were produced using 100 µm thick p-type Si wafers and reached the efficiency of 16.8%[25]. Thin n-type solar cells with whole rear face covered by aluminum achieved the efficiency of 18% and 19% for homogenous and selective phosphorus front surface field[26]. These thin devices showed a bow of ≈ 6 mm after metal firing and needed subsequent thermal step to reduce it.

The aim of this paper is to present the development of thin n^+np^+ silicon solar cells with the p^+ rear emitter formed by boron deposited by spin-on and an Al/Ag grid deposited by screen-printing. Optimization of the metal pastes firing temperature was carried out and results from devices processed with 100 µm are presented and compared to n^+pp^+ thick solar cells. The novelty of this paper is to combine a boron emitter obtained by commercial boron spin-on dopant and thin silicon wafers to produce n^+np^+ solar cells, reaching similar efficiencies than those obtained by thick p-type devices processed with the same fabrication sequence.

2. Materials and Methods

Solar grade silicon wafers grown by the Cz method, n-type, phosphorus doped, resistivity of 1-20 Ω.cm, doping concentration ranging from $2.2x10^{14}$ to $5.0x10^{15}$ cm^{-3}, <100> orientation were used. The thickness of the wafers was reduced to approximately 100 µm by a chemical etch based on KOH and deionized water. This solution was employed because there is not availability of thin wafers in the market.

Figure 1 shows the device fabrication process flow of the n^+np^+ solar cells developed. The process starts with the anisotropic etch to form micropyramids followed by the standard RCA cleaning. A solution containing boron (PBF20, Filmtronics) was spun-on the face and the wafers were introduced in an oven for evaporation of solvents. The boron was diffused into the one face of the wafer in a quartz tube furnace at 970 °C followed by an oxide growth, process optimized in previous works[27,28]. The SiO_2 layer was etched away from the other face and after RCA cleaning, phosphorus was diffused in a quartz tube in the range of 845 °C to 855 °C by using $POCl_3$ as source in order to achieve sheet resistances (R_{SH}) of around 50 Ω/sq. This sheet resistance is suitable to establish low contact resistivity between screen-printed metal grid and the n^+ region of the solar cell. As reported in an earlier paper, phosphorus has to be diffused after boron to enhance the minority carrier lifetime of the silicon wafers[29]. For thick n^+pp^+ devices, the

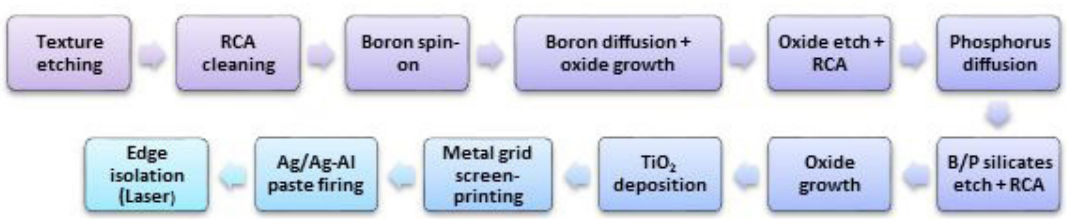

Figure 1. Fabrication process sequence used to produce thin n^+np^+ silicon solar cells.

temperature of 845 °C produced the devices with higher efficiency, but we increased the phosphorus diffusion temperature in this work in order to enhance the gettering mechanism in thin devices, keeping similar sheet resistances for n^+ regions. After that, phosphorus/boron silicate glasses (PSG and BSG) were etched by means of a hydrofluoric acid solution. The boron and phosphorus doped regions were characterized measuring the sheet resistance with the four-point probe technique and the impurity profile with the ECV (electrochemical capacitance-voltage profiling) method[30]. The R_{SH} was measured in 13 regions in the doped wafer. The thickness of the n^+ region and p^+ one as well as the surface impurity concentration (C_S) were obtained from the impurity profile.

To passivate the surfaces, a thin SiO_2 layer was thermally grown at 800 °C[31] and the TiO_2 antireflection coating (ARC) was deposited on the front face. The rear metal grid based on Al/Ag paste (Solamet PV3N1, from DuPont) was screen-printed and this grid has the double function: to contact the silicon wafer and produce the selective BSF region. In the non-metal covered regions on the rear face, the BSF effect is produced by boron doped region previously diffused.

On the front face, Ag grid was screen-printed (Solamet PV17A, DuPont). The pastes were dried in a belt furnace and were fired in the temperature range of 820 °C – 890 °C. The optimum firing temperature is of around 860 °C to process n^+pp^+ solar cells with a thickness of 180 μm[12]. For instance, Sheoran et al.[32] reported that the temperature of 115 μm thick wafers was 70 °C higher than that of 280 μm thick ones, for the same belt furnace temperature. Do et al.[25] and Schiele et al.[26], that developed 100 μm thick devices, did not comment about the firing temperature used.

After the metal grid deposition, edge isolation was performed with laser radiation.

The devices were characterized under standard conditions (100 mW/cm^2, AM1.5G and 25 °C) in a class AAA solar simulator (CT150AAA, PET-Photoemission) calibrated with a silicon solar cell previously measured at CalLab - FhG-ISE (*Fraunhofer-Institut für Solare Energiesysteme*), Germany. Cells had an area of 61.58 cm^2 (pseudo-square of 80 mm x 80 mm) with a standard two-busbars. Figure 2 shows the baseline structure and one thin solar cell produced. The solar cells with higher efficiency were characterized by measuring the spectral response and spectral reflectance (PV300 system, Bentham) in order to obtain the internal quantum efficiency (IQE). One n^+np^+ device was also analyzed by light beam induced current technique (LBIC)[33]. The solar cell was irradiated with laser radiation of four wavelengths (648 nm, 845 nm, 953 nm and 973 nm) and the minority carrier diffusion length (L_D) was estimated.

3. Results and Analysis

The doped regions presented an average sheet resistance of $R_{SH\text{-}Phosphorus}$ = (58 ± 5) Ω/sq for phosphorus diffusion at T = 845 °C, $R_{SH\text{-}Phosphorus}$ = (51 ± 2) Ω/sq for T = 855 °C and $R_{SH\text{-}Boron}$ = (59 ± 4) Ω/sq, values suitable to the metal pastes based on Ag (n^+ face) and Ag/Al (p^+ face). Figure 3 shows the phosphorus and boron doping profiles. The surface phosphorus concentration is of around 1x10^{21} cm^{-3} and the thickness of the n^+ region is in the range from 0.31 μm to 0.40 μm,

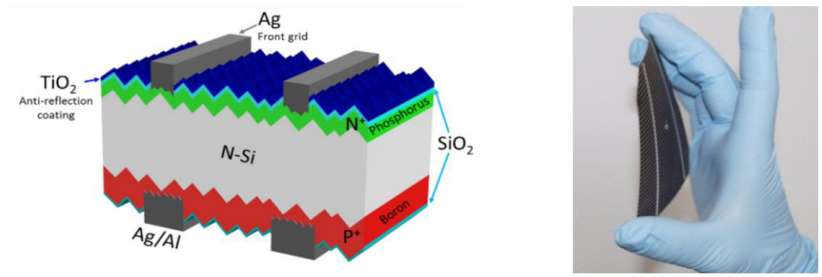

Figure 2. (a) Scheme of the solar cell with rear emitter and (b) thin device processed.

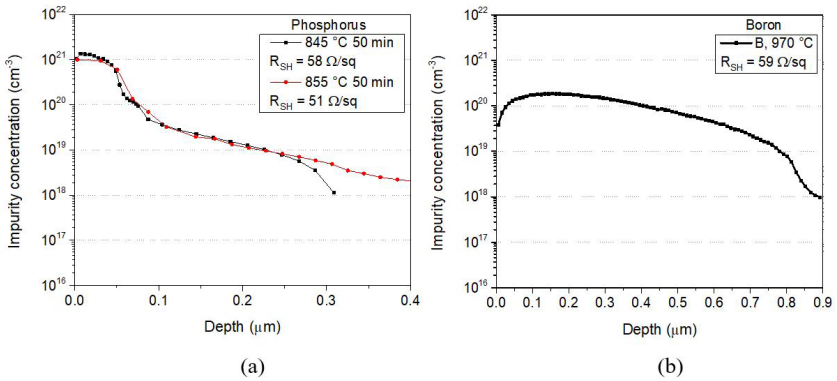

Figure 3. (a) Phosphorus and (b) boron impurity concentration obtained by ECV.

as Figure 3a shows. The boron surface concentration is of around $4x10^{19}$ cm^{-3} and the junction depth is of approximately 0.9 μm (Figure 3b). The depletion of the B concentration close to the surface is due to the impurity segregation to the oxide layer grown during post-oxidation step after boron diffusion and during the phosphorus diffusion.

Table 1 presents the average electrical parameters of solar cells: open circuit voltage (V_{OC}), short-circuit current density (J_{SC}), fill factor (FF) and the efficiency (η) of the devices. The average values were calculated from the results of at least five solar cells. The higher average efficiency was achieved in the range of firing temperature from 840 °C to 860 °C. For the lower firing temperatures, the efficiency standard deviation is enhanced due to the less effective etch-through of the TiO_2+SiO_2 layer by Ag paste.

Table 2 summarizes the electrical characteristics of the devices with the highest efficiency for each firing temperature. The higher efficiencies were obtained at 830 °C and 840 °C. The latter was considered the best firing temperature taking into account the average values presented in Table 1. Moreover, the large efficiency deviation of 2% (absolute) observed when T_{Firing} = 830 °C shows that the firing of the Ag and Ag/Al pastes in this temperature did not establish an ohmic contact with enough reproducibility.

Figure 4 shows the J-V characteristics of the thin n^+np^+ devices that reached the highest efficiency and one thick n^+pp^+ device. The Ag and Ag/Al pastes of thin devices were fired at 840 °C. The p-type Cz silicon wafers, boron doped, with similar resistivity of 1-20 Ω.cm, were supplied by the same company that produced the n-type wafers. The results from thin solar cells presented in Figure 4 show that those cells reached higher J_{SC} than thicker one, that we attributed to effective light trapping and a high bulk minority carrier diffusion length.

In the Figure 5, the internal quantum efficiency (IQE) of the devices with higher conversion efficiency (η) is presented. The surface passivation applied to the solar cells were the same, a SiO_2 thermally growth, but the thicker n^+pp^+ one showed higher IQE for short wavelengths, as predicted by simulating the devices with the computer program PC-1D[34] and setting the surface recombination velocity of 10^5 cm/s for the n^+ front surface. It is worth commenting that in the n^+np^+ structure the electron-holes generated by the solar radiation that is absorbed at the front surface need to be collected at the rear of the cell, where the pn junction is formed.

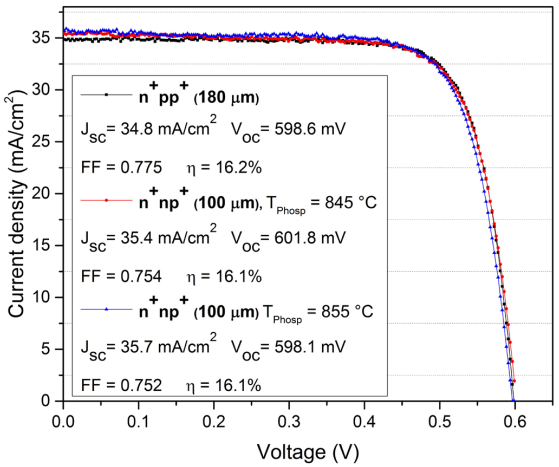

Figure 4. Current density as a function of the voltage of the n^+np^+ thin cells and n^+pp^+ thick standard device. T_{Phosp} is the phosphorus diffusion temperature.

Table 1. Average open circuit voltage (V_{OC}), short-circuit current density (J_{SC}), fill factor (FF) and efficiency (η) of thin solar cells processed at different firing temperatures (T_{Firing}).

T_{Firing} (ºC)	V_{OC} (mV)	J_{SC} (mA/cm²)	FF	η (%)
820	595 ± 5	34.6 ± 1.1	0.71 ± 0.05	14.6 ± 1.3
830	590 ± 12	34.1 ± 1.6	0.70 ± 0.09	14.2 ± 2.0
840	594 ± 5	34.4 ± 1.0	0.73 ± 0.02	15.0 ± 0.7
850	594 ± 2	34.7 ± 0.2	0.74 ± 0.01	15.2 ± 0.3
860	590 ± 1	34.5 ± 0.4	0.74 ± 0.01	15.1 ± 0.2
870	584 ± 1	34.5 ± 0.4	0.73 ± 0.01	14.7 ± 0.2
880	577 ± 5	33.7 ± 0.3	0.70 ± 0.02	13.6 ± 0.5
890	573 ± 4	33.5 ± 0.2	0.70 ± 0.02	13.4 ± 0.3

Table 2. Electrical characteristics of the thin devices with the highest efficiency obtained at different firing temperatures (T_{Firing}).

T_{Firing} (ºC)	V_{OC} (mV)	J_{SC} (mA/cm²)	FF	η (%)
820	600.5	35.7	0.74	15.8
830	600.9	35.2	0.75	16.0
840	601.8	35.4	0.75	16.1
850	593.0	35.4	0.75	15.8
860	591.6	34.8	0.75	15.3
870	585.3	34.6	0.73	14.9
880	576.7	34.0	0.71	14.0
890	576.7	33.3	0.72	13.8

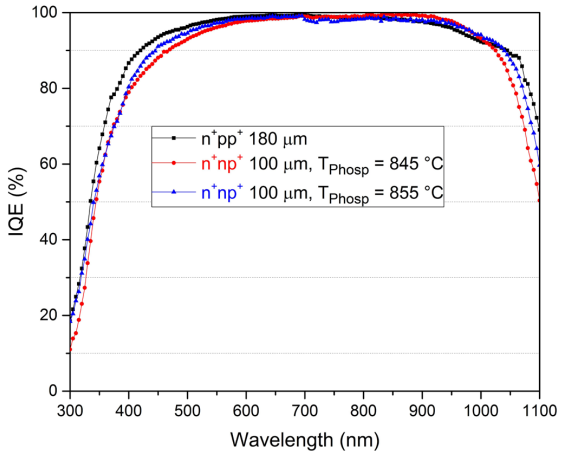

Figure 5. Internal quantum efficiency (IQE) of n^+np^+ thin solar cells with the highest efficiency and of the n^+pp^+ thick standard device.

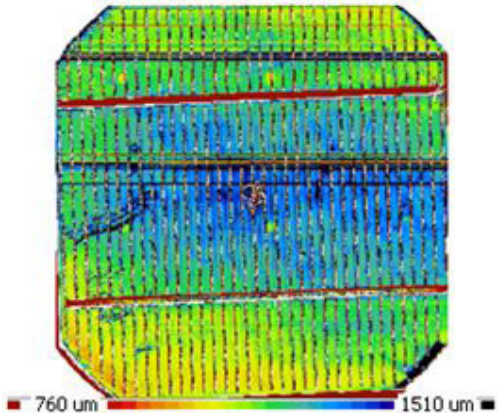

Figure 6. Two-dimensional distribution of the minority carrier diffusion length of the thin n^+np^+ solar cell ($L_{DAverage}$ = 1200 µm). Phosphorus diffusion was performed at 855 °C; T_{Firing} = 840 °C.

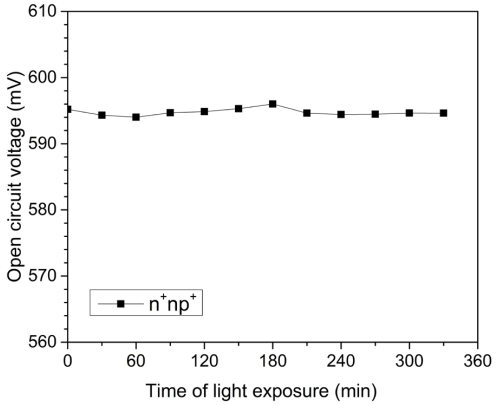

Figure 7. Open circuit voltage of a n^+np^+ thin solar cell as a function of irradiation time. The device was exposed in a steady sun simulator, set to 1000 W/m² (AM 1.5G).

In order to estimate the internal front reflectance (ρ_{fi}) and the rear reflectance (ρ_r), the solar cells were simulated by using the PC1D program and these parameters were adjusted to fit in well the simulated IQE and hemispheric reflectance at longer wavelengths (1000 nm - 1100 nm) to the experimental ones. The ρ_{fi} and ρ_r are the reflectance when the solar radiation impinges on the front and rear face, respectively, from inside the device. The solar cells have the front surface coated with SiO_2/TiO_2 film and the rear face coated by SiO_2. The best fit between experimental and simulation results was found with ρ_{fi} and ρ_r equal to 0.95. These values are similar to those presented in works that deal with light trapping in silicon wafers textured with random pyramids[35]. Although the thickness of the device was reduced about 45%, thinner solar cells presented an IQE (at 1100 nm) approximately 10% lower than thick ones. Therefore, thin textured silicon wafers with the above mentioned films can produce efficient light trapping.

Figure 6 illustrates the distribution of the minority carrier diffusion length obtained by the LBIC technique of the thin n^+np^+ device with P diffused at 855 °C and T_{Firing} = 840 °C. The average value of the diffusion length ($L_{DAverage}$) was of around 1200 µm, that is, twelve times the wafer thickness and corresponds to the high minority carrier lifetime of around 1.1 ms[9,14].

Concerning the lower fill factor achieved by n^+np^+ solar cells with Ag/Al rear metal grid, this is an issue of n-type devices, as observed by Singha and Solanki[14]. To reduce the series resistance of the Ag/Al metal grid, electroplating could be used to augment the finger thickness, but an additional process step would be not cost-effective.

The n^+np^+ thin device, whose J-V is presented in Figure 4 (P diffusion at 855 °C; T_{Firing} = 840 °C), was exposed in a sun simulator, set to 1000 W/m² (AM 1.5G), during 330 min in order to evaluate the light induced degradation. After every 30 min, solar cell was characterized by measuring the J-V curve at standard conditions and no degradation was observed. Figure 7 presents the V_{OC} measured during this period and small deviations from the initial value, less than 2 mV, were observed. As expected, n-type wafers did not present light induced degradation.

4. Conclusions

As observed by ITRPV 2018 report[2], efforts have to be made in the next years to use the crystalline silicon more efficiently and to improve the solar efficiency without significantly rising processing costs. Cost-effective silicon solar cells were fabricated by using 100 µm thick wafers and efficiencies of around 16% were obtained. The firing thermal process of the Ag and Ag/Al metal pastes were optimized and the higher efficiencies and the lower standard deviation of the average values were observed when the firing temperature was of 840 °C. The thin n^+np^+ solar cell was exposed to solar irradiation and no degradation was observed after 5.5 h. Concerning the silicon amount to produce each watt, the developed thin n^+np^+ device can achieve the value of 1.6 g/W, about 40% lower than the obtained in standard n^+pp^+ thick solar cells processed with the same fabrication sequence.

Acknowledgments

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