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A differential IR-UWB transmitter using PAM modulation with adaptive PSD

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Abstract
The current state of the telecommunications market exhibits a high potential to absorb efficient innovations in wireless connectivity, especially those that can be applied to the Internet of Things and similar domains. Contributing in that direction, this paper describes the design and implementation of a fully differential impulse-radio ultra-wideband (IR-UWB) transmitter using pulse-amplitude modulation, with an adaptive power spectrum density (PSD). The architecture can produce up to eight differential monocycles per clock pulse at its output. The number of monocycles controls the bandwidth (thus the PSD) in the mask of IR-UWB technologies, allowing adaptation to multiple standards. The complete transmitter has four main blocks: (a) a pulse generator, comprising two pulse generating circuit groups, to modulate and create a rectangular waveform; (b) an active balun with two amplifiers, to generate differential signals; (c) a digital demultiplexer, to alternate data to the pulse generating circuit groups; (d) a binary-to-thermometer decoder, to control the amount of generated monocycles per pulse. Simulations demonstrate an output pulse amplitude of 120 mV for the high logic level and of 70 mV for the low logic level, both at a 100 MHz Pulse Repetition Frequency. This produces a mean pulse duration of 277 ps, a mean central frequency of 3.8 GHz, and a mean power consumption 6.7 mW. The transmitter takes the form of an intellectual property core in a 130 nm CMOS technology. The complete transmitter area is 0.067 mm^2, without I/O pads. The outcomes suggest that the proposed circuit can narrow or widen the output signal bandwidth, providing adaptability to different emission requirements.

Keywords IR-UWB · PAM modulation · Microwave transmitters · Active balun · IoT · CMOS

1 Introduction and related work

Wireless connectivity is a major enabler technology for the Internet of Things (IoT) [1–3]. The IoT, together with domains with similar requirements, such as wireless sensor networks [4], wearable devices, and mobile health applications [5] further the demand for efficient short-range communication circuits. Advances in the efficiency of such circuits are possible due to the relentless evolution in silicon technologies, which now allow the easy development of Systems-on-Chip (SoC) and wireless technologies integrated into a single silicon wafer [6].

In the short-range communication arena, several researchers believe the Impulse-Radio Ultra-Wideband

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(IR-UWB) is an excellent alternative for many IoT applications, e.g. [4, 7, 8]. IR-UWB has remarkable wireless connectivity and low power consumption, presents high transfer rates, a simple architecture, and low cost. The basic architecture of an IR-UWB transmitter can be implemented using four building blocks, as Fig. 1 depicts: (i) a modulator that encodes the binary input data using an external clock; (ii) a pulse generator with pulse output in the sub-nanosecond range; (iii) amplifier circuits; (iv) a driver for 50 Ω antennas [6].

IR-UWB components can support many applications in environments where the distance between communicating devices is minimal [5]. For example, IR-UWB is effective in home and small office environments, allowing unique communication channels with low power. Other advantages of IR-UWB components include the rejection of multipath fading and security against interception and jamming.

Moreover, there are various carrierless modulation schemes developed for UWB systems for data transmission, including Pulse Amplitude Modulation (PAM), Pulse Position Modulation (PPM) [9], Binary Phase Shift Keying (BPSK) [10], and On-Off-Keying (OOK) [11] which can be designed in different ways. In references [11, 12], authors propose an edge combiner circuit to produce a pulse at the integrated bandpass filter to generate UWB pulses. This technique is straightforward, but presents limitations in generating pulses with different waveforms. Besides, it is also expensive, due to the large area occupied by the required on-die planar inductors and capacitors. Mercier et al. [13] proposed a pulse generator using a single NAND gate to generate a voltage pulse that is applied across an on-chip nMOS-type capacitor and produces a current-voltage relationship like the first derivative (i. e. a monocycle pulse). Besides, Gozalpour et al. propose a transmitter based on the pulse synthesizing technique [14]. This technique is straightforward to apply, but depends on the time control provided by a chain of inverters, composed by a Voltage-Controlled Delay Line (VCDL) circuit, where a rising edge is propagated through tunable delay cells. Finally, Maymandi–Nejad and Sachdev describe an all-digital transmitter implemented with dual, capacitively coupled pulse-shaping drivers [15].

This paper proposes an IR-UWB transmitter using PAM modulation capable of adapting the Power Spectral Density (PSD) to different emission masks. The number of monocycles per pulse controls the bandwidth, enabling to change the PSD profile. By increasing or decreasing the number of monocycles per pulse (from 1 to 8 monocycles), the PSD profile can be modulated for a narrower or wider bandwidth, respectively, as Fig. 2 depicts. The main goal is to architect and design a transmitter circuit using the PSD adaptability concept [16]. The use of a differential output is an alternative to implement the IR-UWB transmitter. This choice enables to achieve high output swings at the transmitter output and to obtain high gain and thermal noise reduction.

Section 2 presents the architectural description of the transmitter circuit in detail. Simulation results and the process of the circuit layout generation are the target of Sect. 3, followed by conclusions and ongoing work, in Sect. 4.

This article extends a previous work of the Authors [17]. The architecture proposed in [17] is enhanced here to become a complete differential IR-UWB transmitter. Section 2.4 describes an active balun block, included to enable differential pulse generation. Also, the transmitter is redesigned at the layout level, a topic covered in Sect. 3.

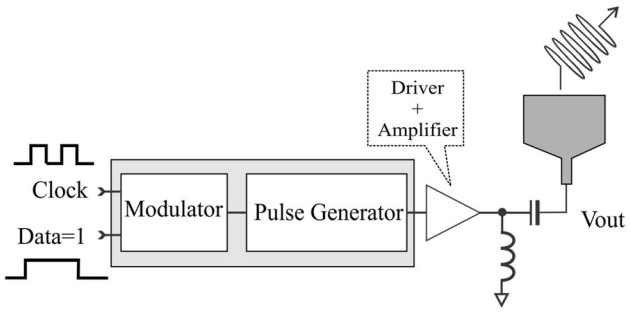

Fig. 1 A generic block diagram of an IR-UWB transmitter comprising four building blocks: a modulator, a pulse generator, an amplifier, and an output driver

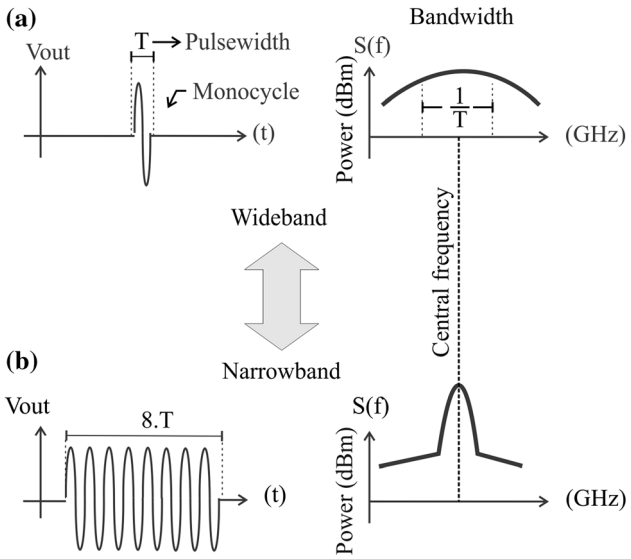

Fig. 2 Waveforms and power spectral density of pulses with different monocycles per pulse: **a** a single-monocycle pulse and a wideband spectrum; **b** an eight-monocycle pulse and a narrowband spectrum

2 The transmitter architecture

The IR-UWB pulse generator proposed here uses a PAM modulation scheme to produce two pulse amplitude variations at the output to represent either the high or low logic levels at the input. The pulse requires only a single polarity to represent a data signal: high amplitude represents a high logic level, while low amplitude represents the low logic level. Additionally, each pulse at the output of the pulse generator can contain up to 8 monocycles per pulse to adapt in the target PSD emission mask, as Fig. 3 shows. This circuit is implemented with four main blocks:

1. *Demultiplexer block* enables the clock transmission to the Edge Combiner High (ECH) or Edge Combiner Low (ECL) blocks. This circuit requires two AND gates (G1 and G2) and an inverter gate;
2. *Pulse generator block* eight pulse generator units (PGU) connected in parallel. Each PGU uses two edge combiner circuits (ECH and ECL) for generating high amplitude (ECH) or low amplitude (ECL) monocycles, regarding the PAM modulation scheme. Thus, the 8 PGUs can produce 1 to 8 monocycles per pulse. A biased filter is connected to the output of the PGU parallel association;
3. *Binary-to-thermometer decoder block* a digital block responsible for selecting the PGUs, changing the number of monocycles per pulse;
4. *Active balun block* The balun block is responsible for transforming a single-ended signal to a differential signal [18].

The operation mode of the pulse generator is relatively simple, based on the binary input *Data*. Referring to Fig. 4, when *Data* is set to high, the clock signal goes to the ECH PGUs (*ck1* in Fig. 4(a)), otherwise it goes to the ECL PGUs (*ck2* in Fig. 4(b)). Then, the *Binary-to-thermometer Decoder Block* selects the number of monocycles at the output pulse. This monocycles-selection defines the number of PGUs used to generate the pulse at high or low amplitude. Then, the pulse is connected to the output biased filter to shape the oscillations. The following sections detail the design main blocks.

2.1 Demultiplexer block

The decision circuit is implemented with a 1:2 Demultiplexer (DEMUX) circuit using two static CMOS NAND gates, and an inverter gate to select the output, as shown in Fig. 4(a, b).

2.2 Pulse generator block

The proposed pulse generator block contains 8 PGUs to produce up to eight monocycles per clock pulse at its output, as Fig. 5 shows. Each PGU has two Edge Combiners (EC), adapted from [17]. Each EC (ECH or ECL) uses pMOS and nMOS transistors connected in series. Table 1 presents the widths of the transistors appearing in Fig. 5.

To generate the monocycles at the pulse generator output, each EC requires two delay circuits to produce a small

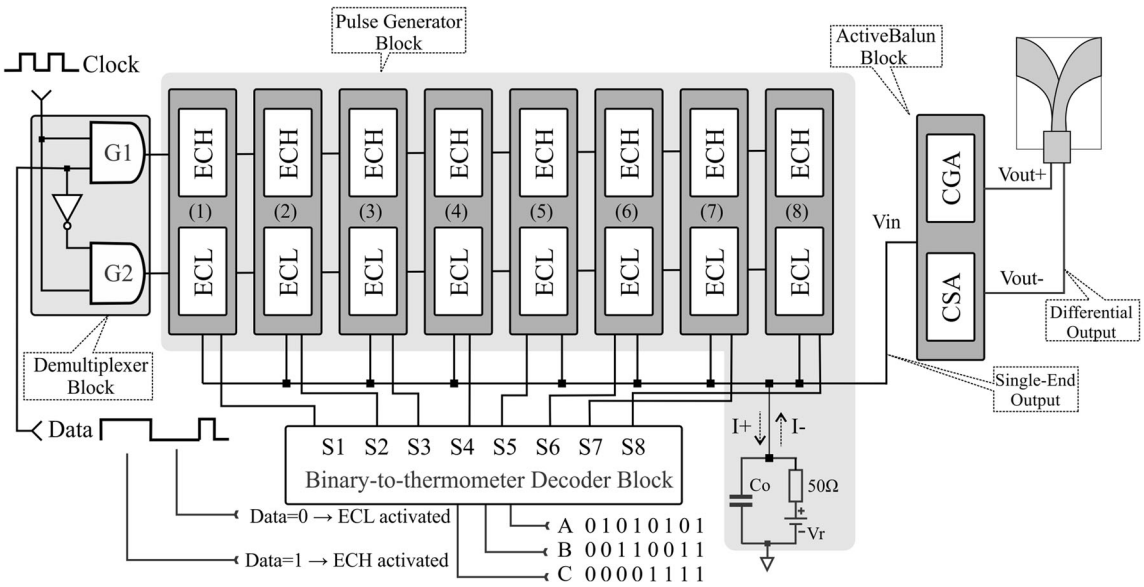

Fig. 3 The detailed architecture of the implemented IR-UWB transmitter highlights the four main constituent blocks: demultiplexer, pulse generator, binary-to-thermometer decoder, and active balun

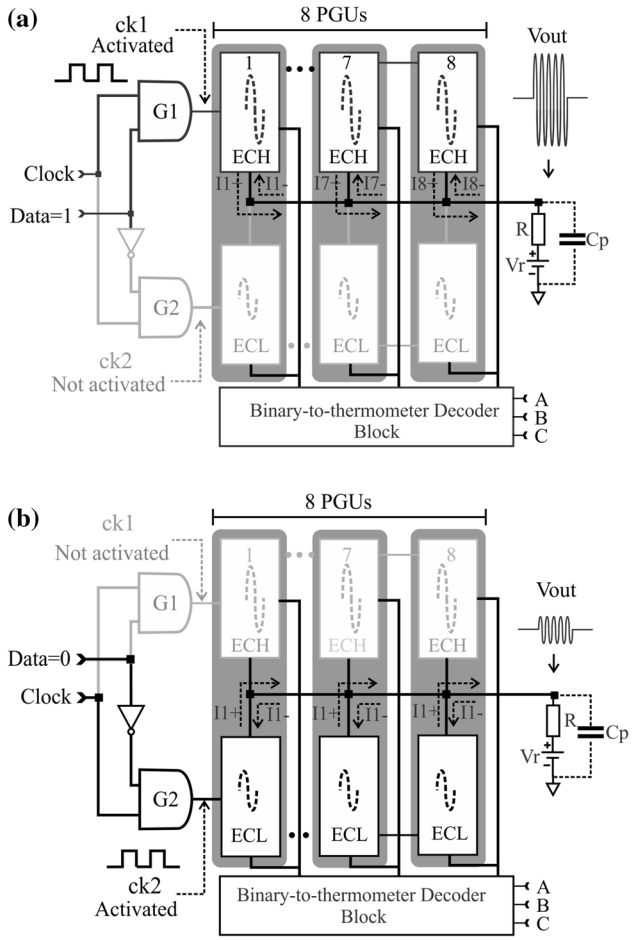

Fig. 4 The operation mode of the pulse generator: **a** when *Data* = 1, ck1 and ECH are activated; **b** when *Data* = 0, ck2 and ECL are activated

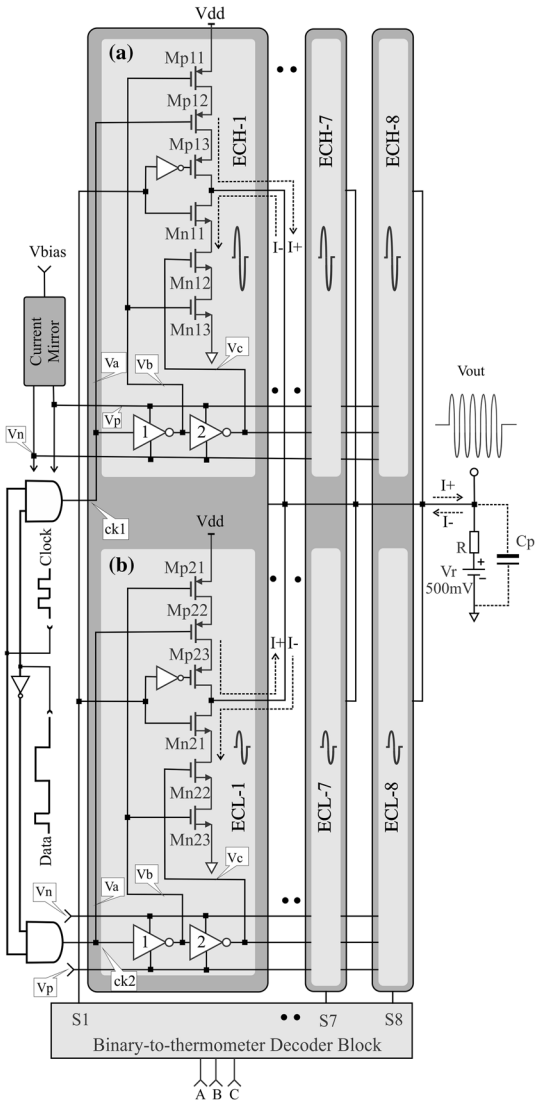

Fig. 5 Diagram of the pulse generator with eight pulse generator units (PGU) using pulse amplitude modulation (PAM) scheme. The PGU-1 is presented in detail: **a** shows the edge combiner high (ECH-1), and **b** shows the edge combiner low (ECL-1)

current pulse in the biased capacitor that converts into a voltage pulse, as Fig. 5 shows. The EC operation consists of connecting a square clock pulse train Va on the first PGU with a Pulse Repetition Frequency (PRF) at the input of the first delay circuit. As a result, a pulse Vb is generated with a short time delay (Δt) between input and output. A narrow current pulse (I+) is generated at the EC output with a width of Δt and its current flows from Vdd through the biased capacitor to the Gnd. This pulse occurs when the pMOS transistors are activated through voltages Va and Vb. A similar process takes place when a negative current pulse (I−) is generated at the EC output. The phase difference between Vb and Vc signals causes such a pulse. Signals Va and Vb generate the positive peak voltage of the monocycle through the following states:

1. First state, before transition: suppose that signals Va='1' and Vb='0'; then (I+)='0'. Under this condition, Mp11 is on and Mp12 is off;
2. Second state: when Va goes from '1' to '0', and Vb goes from '0' to '1', Mp11 and Mp12 go on, generating a narrow current pulse; then the current (I+) flows from Vdd to Gnd, through the biased capacitor;
3. Third state: after the transition, assume signals Va='0' and Vb='1'; then pulse current (I+)='0'. Under this condition, Mp11 is off and Mp12 is on.

The negative peak of the monocycle is generated similarly through the following states:

1. First state, before transition: suppose that signals Vb='0' and Vc='1'; then (I−)='0'. Under this condition, Mn11 is on and Mn12 is off;
2. Second state: when Vb goes from '0' to '1', and Vc goes from '1' to '0', Mn11 and Mn12 go on, generating a narrow current pulse; then the current (I−) flows from Vout to Gnd;

Table 1 Transistor sizes of ECH and ECL circuits presented in Fig. 5

Transistor	Mp11	Mn11	Mp12	Mn12	Mp13	Mn13	Mp21	Mn21	Mp22	Mn22	Mp23	Mn23
Width (μm)	40	13	40	9	9	40	20	7	20	7	20	7

3. Third state: after the transition, suppose that signals Vb='1' and Vc='0', then (I−)='0'. Under this condition, Mn11 is off and Mn12 is on.

When the PGU is not selected by one of the decoder outputs (signals S1 to S8), transistors Mp13, Mn11, Mp23, and Mn21 are off, disabling the output node (high impedance state). However, when the PGU is selected, both ECH and ECL are selected through transistors Mp13, Mn11, Mp23, and Mn21, which are on. When the *Data* signal is high, just ECH is selected to generate high amplitude monocycles at Vout, as Fig. 5(a) shows. Conversely, when the *Data* signal is low, just ECL is selected to generate low amplitude monocycles at Vout, as Fig. 5(b) shows. In this block, the monocycle is generated at the output, due to the phase difference among delay signals Va, Vb, and Vc, as Fig. 6 show. Table 2 displays the width of the transistors appearing in Fig. 6.

The delay circuits are a fundamental part of this transmitter, since without the difference between the input and output phases, the monocycle cannot be generated at each PGU output. In the literature, there are several delay circuit proposals e.g. the one described in reference [19]. However, this project implements three inverters in cascade. The choice of these inverter topologies is not only due to their simplicity but also due to their extensive use in VSLI projects. The delay circuits not only have the function of generating pulses, they also have the keep a central frequency of (fixed or variable) operation.

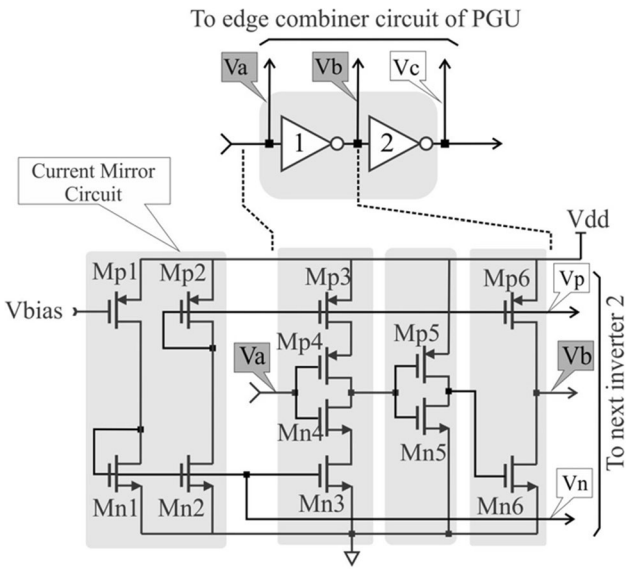

Fig. 6 Schematics of the delay circuit

The first inverter of the delay circuit (Fig. 6) employs a current-starved topology with symmetrical load (Mp3 and Mn3) to control the current over Mp4 and Mn4 [16, 20, 21]. This type of inverter performs a frequency adjustment through two current mirror circuits. One of these is the type N current mirror, whose transistor Mn1 has the drain and gate shorted (diode connection). This transistor is also connected in series with transistor Mp1, whose function is to control the passage of current through the voltage Vbias. The Mn1 gate is also connected to transistor Mn2 gate and the symmetrical load (Mn3) of the current-starved inverter [22]. In the type P current mirror, transistors Mn2 and Mp2 are connected to replicate the current control on the P side. Thus, Mp3 and Mn3 handle the current on the inverter formed by Mp4 and Mn4. It is thus possible to control the rise and fall times of voltages Va, Vb, and Vc, which are connected to the EC.

The second inverter is a conventional-type inverter (Mp5 and Mn5), connected in series with the predecessor inverter (current-starved inverter). It is necessary to compose an odd number of inverters in the delay circuit also contributing to increase the total delay.

Finally, the third inverter (Mp6 and Mn6) uses a pseudo-nMOS topology [16]. This type of inverter has the Mp6 transistor operating as an active load connected to the Mn6 transistor. Figure 6 shows transistor Mp6 connected to the current mirror type P. It is thus possible to produce a current proportional to the transistor dimension and to the gate voltage provided by the Mp2 current mirror. The output signal of this inverter (Vb) is connected to a second delay circuit, and also to the EC nMOS/pMOS respective transistors. There is then an increase in capacitive load and, consequently, more significant propagation delay and rise times. The current peak amplitude generated at the EC output and the operational transmitter frequency are proportional to the delay circuit delay.

2.3 Binary-to-thermometer decoder block

The Binary-to-Thermometer Decoder (BTD) circuit has been used for a long time in electronic circuits, mainly in analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) [23]. To meet the requirements of an ADC circuit, the BTD is implemented with operational

Table 2 Transistor sizes of delay circuit presented in Fig. 6

Transistors	Mp1	Mn1	Mp2	Mn2	Mp3	Mn3	Mp4	Mn4	Mp5	Mn5	Mp6	Mn6
Width (μm)	5	3	5	3	4	2	4	2	2	1	10	5

Table 3 Binary-to-thermometer coding for choosing the number of monocycles per pulse (from 1 to 8 monocycles per pulse). Each pulse generator unit (PGU) is responsible for generating one monocycle

BCD	Thermometer code to activate PGUs							
	S1	S2	S3	S4	S5	S6	S7	S8
000	1	0	0	0	0	0	0	0
001	1	1	0	0	0	0	0	0
010	1	1	1	0	0	0	0	0
011	1	1	1	1	0	0	0	0
100	1	1	1	1	1	0	0	0
101	1	1	1	1	1	1	0	0
110	1	1	1	1	1	1	1	0
111	1	1	1	1	1	1	1	1

amplifier circuits to compare an analog signal with successive reference voltages. There are also versions of BTD implemented with combinational logic circuits [24]. Despite both being efficient, this work chooses the digital version for its straightforward implementation (with AND and OR logic gates) and low power consumption, when compared to the analog version. In this project, BTD selects how many PGUs are activated (up to eight PGUs per pulse). With this, it is possible to change the power level of the transmitted signal. This work implements 8 PGUs but the amount can easily be changed to any other. However, the number is limited to the PRF, so that the sum of each monocycle period does not exceed it.

The BTD block is implemented to select the number of monocycles per pulse, as shown in Table 3. Each PGU is connected to the output when its input (S) goes to high logic level, as shown in Fig. 5. For example, when S1='1', transistors Mp13 and Mn11 of ECH and Mp23 and Mn21 of ECL are on. When S1='0', these transistors are off, and the PGU is in high impedance state. Thus, when a binary input "000" is applied to the BTD block, the thermometer output goes to "10000000" (S1='1') connecting the first PGU to the output, while other PGUs are in high impedance state (S2-S8='0'). Under this condition, just one PGU is activated, and one monocycle is generated at the output of the pulse generator block. When the binary input is "111", all eight PGUs are activated (S1-S8='1'), and eight oscillations per pulse are generated.

2.4 Active balun block

In the area of radio-frequency, balun circuits are widely used to convert differential signals to single-ended or vice-versa and to phase out the output signals [25] by 180 degrees. An active balun is implemented with active components such as differential amplifiers, cascading common source (CS)—common gate (CG) amplifiers, among others. A passive balun is generally built with LC–LC networks, and planar transformers [26, 27]. However, passive baluns can have many parasitic effects, degrading

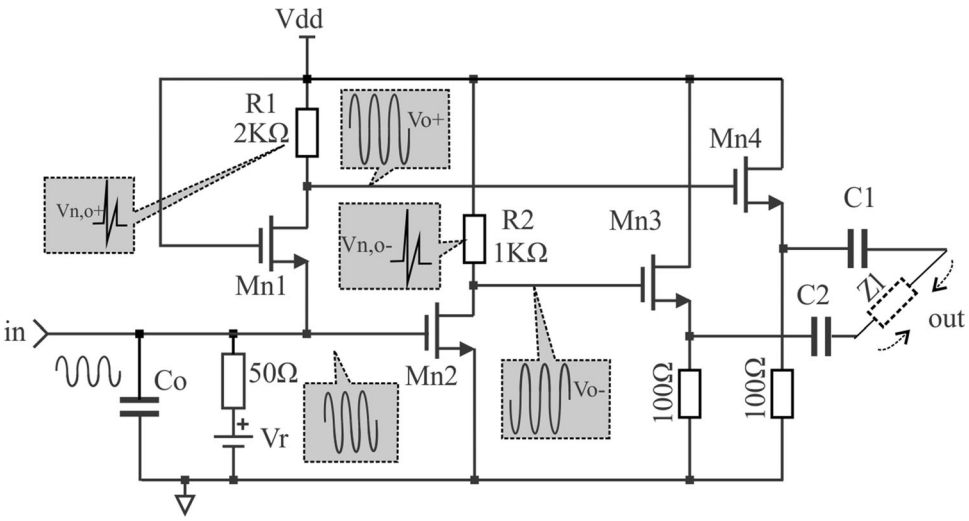

Fig. 7 Active balun implemented with common-source (CS), common-gate (CG) and common-drain (CD) amplifier topologies

Table 4 Transistor sizes for the active balun from Fig. 7

Transistors	Mn1	Mn2	Mn3	Mn4
Width (μm)	20	5	50	50

the performance of the component. Finally, the large area of passive components, combined with other difficulties, make passive baluns an unattractive option. The active topology presents some advantages, such as noise cancellation and area reduction [28–32].

In the CS topology, the input signal is at the transistor gate, with a high input impedance. However, when these amplifiers operate at high frequencies, gain problems arise due to the gate capacitances and the characteristics of the input signal, resulting in a reduction in the amplifier's gain [33]. Miller's effect is another phenomenon present in this type of amplifiers.

The CG amplifier does not have the issues with parasitic capacitances [34], due to the low input impedance (inversely proportional to the transistor transconductance [33]). Thus, this amplifier can operate at much higher frequencies than the CS amplifier. However, a balanced gain from the outputs when compared to the input is not easily obtained.

Neither CS nor CG use the "peaked" technique to extend the transistors passband. They are optimized to operate with frequencies in the order of a few GHz, because the high-frequency operation of conventional CS and CG amplifiers degrades the amplitude and phase of the output signal [35].

The active balun design used here consists of three stages to generate differential pulses at the output of the device, as shown in Fig. 7. Table 4 presents the width of the transistors appearing in Fig. 7. The next items details each balun stage:

1. The first stage consists of two amplifier topologies: one CS and one CG [36]. The CS amplifier operates as a voltage amplifier and provides a 180-degree phase shift at the output. In this amplifier, the gate of Mn2 is the input and is connected to the pulse generator output. The drain terminal is the circuit output and is connected to the R2 resistance of 1 kΩ. The CG amplifier does not change the signal phase at the output, as the input signal is connected at the source terminal and the drain terminal is connected to the R1 resistance of 2 kΩ;
2. The second stage consists of two common-drain (CD) amplifiers operating as an output buffer, as they have a very high input impedance and low output impedance, as shown in Fig. 7. In this amplifier, the transistor gate terminal is connected to the output of the CS and CD amplifiers. The main advantages of this structure are the noise cancellation between amplifiers (differential output) [35, 37] and the supply current feature to the loads. At the output, 100 Ω resistors are connected to the amplifiers;
3. The third stage consists of 5 pF decoupling capacitors C1 and C2 that are connected to the output of the CD amplifiers, as shown in Fig. 7. These capacitors are designed to eliminate the DC level of the output signal.

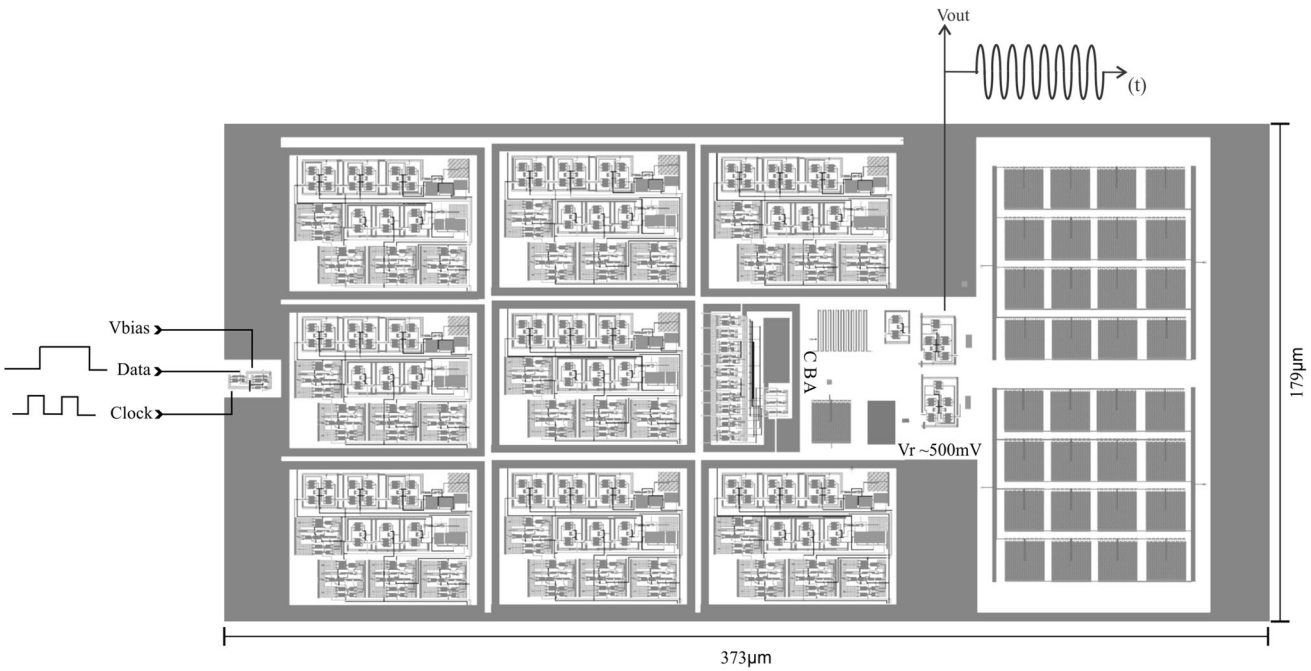

Fig. 8 Complete layout of the proposed transmitter, without PADs

Table 5 Comparative summary of IR-UWB pulse generators and transmitters

Results	This work	[5]	[9]	[21]	[27]	[40]	[39]
CMOS tech. (nm)	130	180	130	180	180	180	90
Supply voltage (V)	1.2	1.8	1.2	$\sim$ 1.8	1.8	1.2	1
Method	EC	LO-based	Filtered EC	Filtered EC	LO-based	Double PLL	Filtered EC
Area (mm^2)	0.067	0.2	0.54	0.09	0.55	0.04	0.18
PRF (MHz)	100	40.5	100	100–1000	125	31.25	860
Power (mW)	6.7	1.97	3.84	0.26–0.76	4	5	12.13
Modulation	PAM	PAM	OOK	OOK	PPM + BPSK	OOK	BPSK
Adaptability	Yes (PGUs)	NP	Yes (filters)	Yes	NP	NP	Yes (notch filter)

EC Edge combiner, *LO* Local oscillator, *PLL* Phase locked loop, *PAM* Pulse amplitude modulation, *OOK* On–off keying, *PPM* Pulse position modulation, *BPSK* Binary phase shift keying, *NA* Not available, *NP* Not present

Finally, there is a load resistance (Zl) of 50 Ω connected to the capacitors.

3 Simulation and transmitter layout generation

This section presents the transmitter simulation results using a PRF of 100 MHz and 1. V power supply in a 130 nm CMOS process. Resistors are implemented using poly resistances with a Vdd-biased substrate to avoid noise, while capacitors are created with Metal-Insulator-Metal (MIM) to avoid noise and other parasitic effects. The external 500 mV voltage supply (Vr) is built to bias the PGU output, and output buffers for PAD connections are also present [38]. All simulations are carried out using the LTSpice electrical simulator and the ELECTRIC layout editor. This flow enables to conduct post-layout simulations.

Figure 8 presents the layout without PADs, with an area equal to 0.067 mm^2. The mean power consumption of the pulse generator without driver circuit is 2.9 mW, and the average power consumption of the balun block is 3.2 mW.

Table 5 compares the present work with related approaches, using as criteria technology node, voltage supply, design method, area, PRF, power consumption, modulation technique choice and degree of design

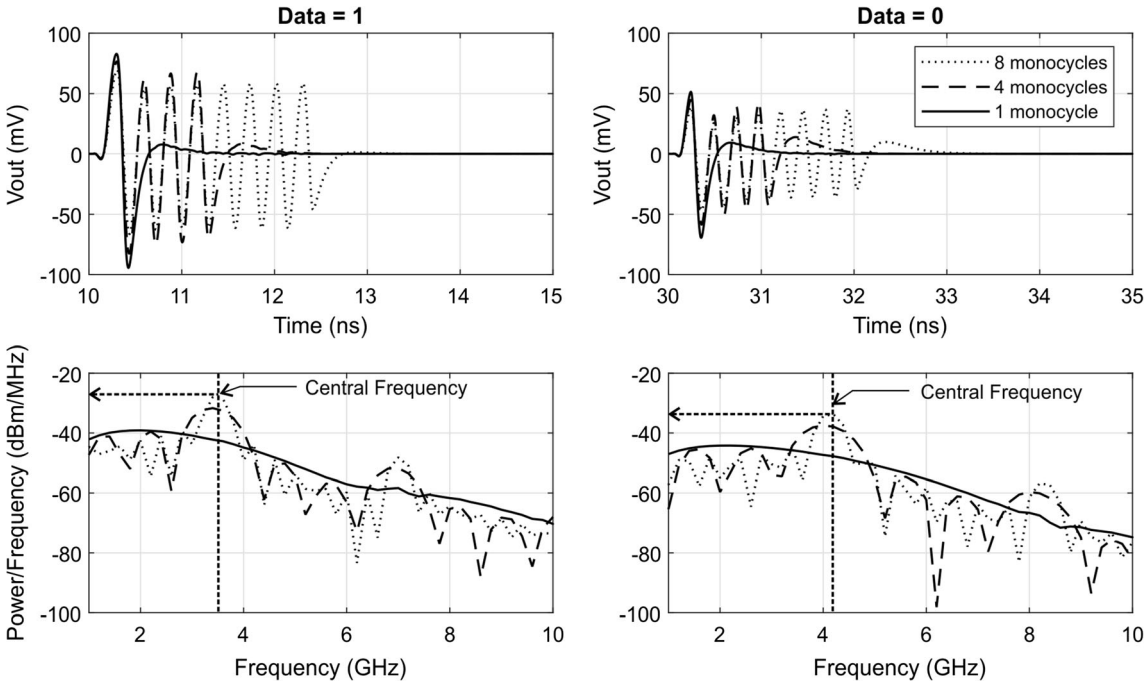

Fig. 9 Power spectrum density (PSD) for *Data* = 0 and *Data* = 1, simulated for 1, 4, and 8 monocycles. Top graphs show the output voltages, while the bottom graphs show their corresponding PSD. Both intervals above are 5 ns in length with a sample rate of 10^{12}. The correspondent DFTs were calculated with the same sample rate

adaptability. This Table shows a comparison between this and other similar designs of transmitters in MOS processes with different dimensions. Due to the diverse structure of the compared circuits, power figures in the Table are not directly comparable. Each work considers a different set of modules composing the block where power is measured, among other discrepancies. For similar characteristics, this project stands out from others in terms of PSD *adaptability*. Most of the approaches in the literature do not have adaptable PSD. While reference [21] reports the support to adaptive PSD in their approach, there is a dependency in that design between PRF and PSD values. These can be independently chosen in the design described here. In [39], the adaptability aims to mitigate the mutual interference between UWB and WLAN systems by having a spectral notch in the transmitted frequency band where the coexistent narrow-band spectrum appears.

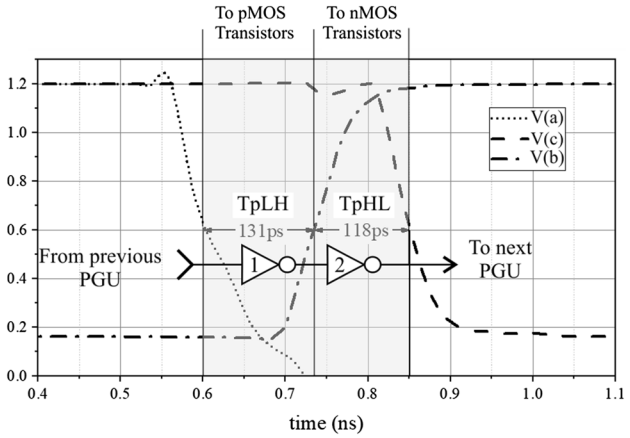

Fig. 10 Waveforms of voltages Va, Vb, and Vc of the delay circuit, showing phase differences

To show how the design proposed here is highly adaptive, Fig. 9 shows a difference between central frequencies. When $Data = 1$, the central frequency is 3.4 GHz and when $Data = 0$ it is 4.2 GHz. This difference is due to the rise and fall times of Va, Vb, and Vc voltages, as shown in Fig. 10. In addition, the dimension of the edge combiners ECH and ECL transistors generates different current amplitudes through the capacitor that produces the voltage at the output of the pulse generator, as shown in Fig. 6. Thus, the times of each monocycle are different and consequently their frequencies differ, due to the relationship between current and time to charge the capacitor. The total duration of the pulse with eight monocycles at the output is 1.66 ns and the total duration of a monocycle is 277 ps. The transmitter circuit output has a pulse amplitude of 120 mVpp for a high logic level and 70 mVpp for a low logic level, as shown in Fig. 11. The PSD obtained with the Discrete Fourier transformation (DFT) is -28 dBm/MHz for the high logic level and -34 dBm/MHz for the low

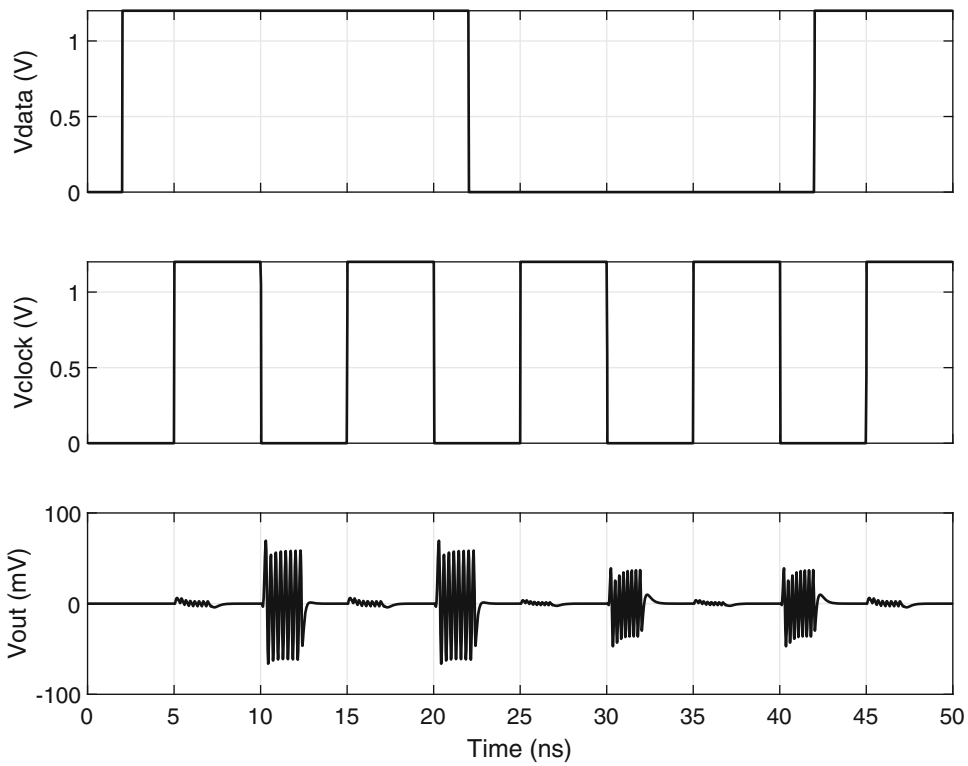

Fig. 11 Time-domain waveforms of the transmitter: the top graph shows data (Vdata); the middle graph shows the clock (Vclock), and the bottom graph shows the differential output (Vout)

level, with a load impedance of 50 Ω at the output of the transmitting circuit, as can be observed in Fig. 4 (a, b).

4 Conclusions

This work discusses the architecture and implementation of an efficient IR-UWB transmitter using PAM modulation, design in a 130 nm commercial CMOS technology. Pulses at the output have an amplitude of 120 mVpp for the high logic level and 70 mVpp for the low logic level, both measured at 100 MHz of PRF. The module produces a mean pulse duration of 277 ps, a mean central frequency of 3.8 GHz, and mean power consumption of 6.7 mW. The full transmitter block occupies an area of 0.067 mm^2. The module presents small area, low power consumption, and low complexity. It is applicable to construct adaptive and reconfigurable circuits for IoT and other domains where wireless communication is a must.

An ongoing work is to complete the architecture to make it available as a send/receive communication module that employs IR-UWB.

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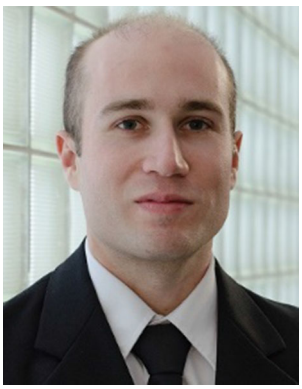

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