Conducted EMI susceptibility analysis of a COTS processor as function of aging

Juliano Benfica, Fabian Vargas*, Matheus Fay Soares, Dorian Schramm

Electrical Engineering Dept., Catholic University – PUCRS, Av. Ipiranga 6681, 90619-900 Porto Alegre, Brazil

A B S T R A C T

This work analyses the conducted electromagnetic interference (EMI) immunity of the Cortex-M4 processor as function of aging. With this purpose, voltage dips were injected in the V_{DD} input power pins of the processor as ruled by the IEC 61000–4-29 standard, whereas aging test was performed by means of the 1015.9 Burn-In Part of the Method MIL-STD-833E. After 456 h of burn-in at 125 °C, the processor presented a current increase in excess of 2.36% and conducted EMI immunity degradation in the order of 158% for the processor operating at extremely low voltage. If the processor is running in the manufacturer's recommended operating voltage range, then such degradation turns into 38%. Moreover, it was measured negligible performance degradation according to the Dhrystone V2.1a benchmark.

1. Introduction

Technology scaling, which made electronics accessible and affordable for almost everyone in the globe, has advanced integrated circuit (IC) and electronics performance since sixties. Nevertheless, it is well recognized that such scaling has introduced new (and major) reliability challenges to the semiconductor industry [1–4]. International standards have been proposed and used to test ICs for aging (such as the Part 1015.9 of the MIL-STD-883H [5]) as well as for conducted and irradiated electromagnetic interference (EMI) [6–9]. Notwithstanding, these standards do not take into account the possible combined effects of aging may have on the immunity level of ICs.

A previous published work [2] addressed the effect of EMI on a commercial micro-controller (whose part number and manufacturer were omitted in the text) according to the Direct Power Injection (DPI) standard [10]. In [4], authors presented an EMC reliability model to predict EM emission of an IC. This model took into account aging due to a combination of high temperature, current, and voltage stresses. The EM prediction model was validated based on a commercial FPGA (Xilinx Spartan 6). In [11], authors presented a modeling methodology aiming at predicting the impact of aging on the susceptibility level of a phase-locked loop (PLL) circuit after an accelerated-life test (due to high temperature). PLL susceptibility was characterized according to the direct power injection (DPI) method defined by IEC 62132–3 standard [10]. Other authors [12,13] published a work that analyzes the combined effects of conducted EMI and total-ionizing dose (TID)

radiation and single-event upset (SEU) in FPGA ICs. However, these works do not focus on understanding how aging interferes on the EM immunity of complex ICs such as the Cortex-M4 processor.

The Cortex-M4 processor, which was designed specifically to target the already crowded microcontroller unit (MCU) market [14,15], has been used not only in high-volume consumer applications, but also in critical/safety applications such as automotive body systems, industrial control and wireless networking, among others. In the specific application of automotive systems, reliable performance is paramount to such highly complex interoperable systems. However, from the best of our knowledge, no work has been published yet addressing the effect of aging on the conducted immunity of the Cortex-M4 processor. Therefore, it is superlative to understand and predict how the component's susceptibility to conducted noise on power bus evolves during lifetime. In this scenario, this paper analyses the effect of aging, by means of burn-in test procedure, on the susceptibility of the Cortex-M4 processor to conducted noise on the V_{DD} input power pins of the chip. The burn-in test procedure was carried out as ruled by the 1015.9 Part of the MIL-STD-883H Method, whereas the conducted EMI test was performed as defined by the IEC 61000-4-29 standard.

2. Case-study platform

Fig. 1 depicts the platform developed to perform the experiment. It was based on the Cortex-M4 processor (part number STM32F303K8T6, Package LQFP32, CMOS 90 nm technology node). In order to minimize
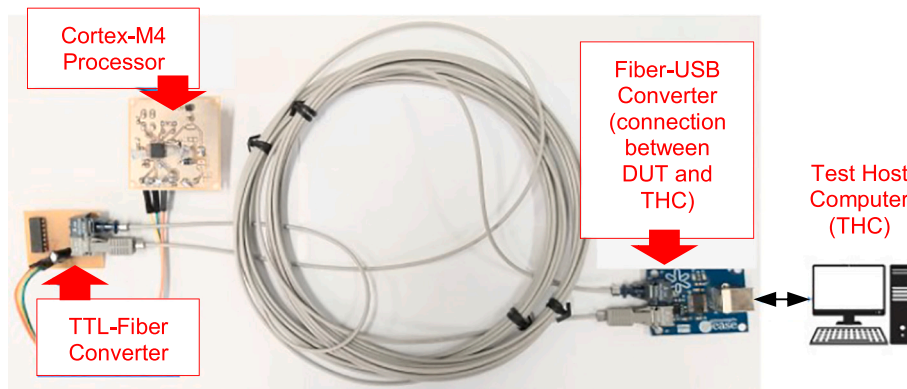

Fig. 1. Test platform.

aging effects on different system components, which could result in a complex analysis, the board was designed having in mind a minimal chipset: only the Cortex-M4 component with a reset circuit, a 20 MHz crystal external oscillator, connectors and decoupling capacitors defined according to the manufacturer's datasheet. The communication between the board and the test host computer (THC) was based on a two-module optic fiber link, where the TTL-fiber converter was connected to the Cortex processor, while the fiber-USB converter was connected to the THC port. We have designed optic fiber connections in order to avoid coupling noise induced by the voltage dips generator on communication cables.

2.1. Embedded software

The selected application software to run on the Cortex-M4 processor was the Dhrystone V2.1a benchmark [16]. This is a well-known application from the designers' community used since the 80's to exercise the entire set of mathematical (integer) instructions and data string manipulations of processors. It is worth noting that the whole code and data were stored in the processor embedded memory (no external memory was available at board level). The output of such application is given in *Dhrystones per second, i.e.*, computed as the number of iterations of the main code loop is performed by the processor per second.

3. Test setup

The test procedure was divided in three steps, as follows:

A. Characterization of the fresh component;
B. Burn-in exposition of the device (Part 1015.9 of the MIL-STD-883H);
C. Injection of conducted EMI in the form of voltage dips on power supply lines of the device (IEC 61000–4-29 std).

3.1. Characterization of the fresh component

Initially, it was determined the "gold" parameters as measured in the fresh device. Later, these "gold" parameters were used as reference values when measuring the device immunity to conducted noise on power supply lines, after each burn-in session.

The component immunity was characterized pre and post burn-in procedures in terms of: (1) current consumption, (2) minimum power supply voltage (V_{DD}) for a correct operation of the component, (3) performance of the component (given in *Dhrystones per second*) when executing the benchmark program, and (4) reliability of the component, measured as function of the number of *observed errors* that were produced by the processor during conducted EM immunity test procedure [6].

3.2. Burn-in test

Burn-in tests were based on the Part 1015.9 of the MIL-STD-833H std. and used a climatic chamber model CSZ MicroClimate [17] able to control temperature in the range [− 20 °C, 180 °C]. In the experiment, we aged the component at a constant temperature of 125 °C in a total of 456 h distributed as follows:

- Day 1: 24 h of burn-in;
- Day 2: 24 h of burn-in;
- Day 3: 24 h of burn-in;
- Days 4–6: 72 h of continuous burn-in;
- Days 7–9: 72 h of continuous burn-in.

As ruled by [5], measurements of the three parameters: current consumption, minimum power supply voltage (V_{DD}) and performance, did not exceed 96 h after every burn-in session. Moreover, during the burn-in experiment the component was powered on with nominal V_{DD} (3.3 V) and executed the benchmark *Dhrystone* in loop mode at a clock frequency of 70 MHz.

3.3. Conducted EMI on the V_{DD} power supply lines

The conducted EMI test was performed by directly applying voltage dips, based on [6], on the V_{DD} power supply pins of the Cortex-M4 processor. For the experiment, on-board voltage regulators were bypassed so that noise was directly injected into the component V_{DD} pins. Voltage dips were applied to the component at a time interval of 5 s, with a pulse duration of 0.01 s, 0.1 s and 1 s (see Fig. 2). These voltage dips were applied to the IC with two different amplitudes, one at a time: (a) 2.0 V down to 1.92 V (namely, the critical amplitude range R1), and (b) 3.3 V
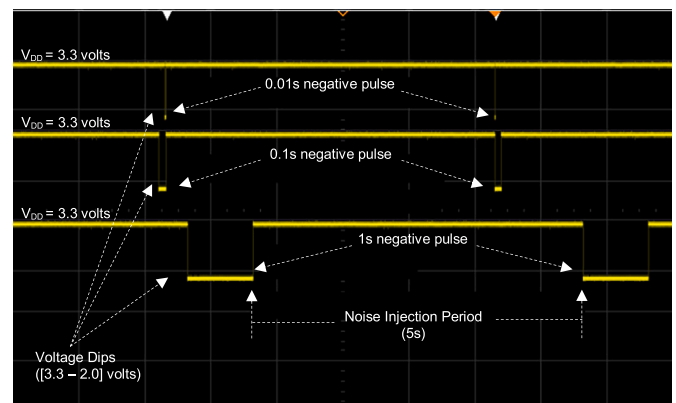
Fig. 2. Oscilloscope print screen of the injected noise in the V_{DD} power pins of the Cortex-M4 processor.

down to 2.0 V (nominal amplitude range R2). R1 and R2 were selected according to the following procedure: (a) we measured the minimum operating voltage for the component and found out to be 1.92 V. At V_{DD} = 1.92 V and clock frequency of 100 MHz, the processor operated correctly; below this value, the processor did not start-up. (b) we checked in the component datasheet the minimum and maximum operating voltages as recommended by the manufacturer (2.0 and 3.3 V, respectively).

The considered voltage dips were generated and applied to the component by means of a digital signal generator combined with an Agilent oscilloscope (Model Agilent DSO-X 3012A). It is worth noting that since the digital signal generator was not able to drive enough current to the processor, a power stage interface was designed and placed at the digital signal generator output. The power interface was built around a high-throughput current operational amplifier (Part Number L2720W13TR) featuring a buffer mode connected at the output of the digital signal generator.

Noise was injected as previously described for the Cortex-M4 processor running at four different clock frequencies: 100 MHz, 70 MHz, 35 MHz and 10 MHz. Fig. 2 depicts the injected noise.

Consider also aging influence on other passive components, such as capacitors and resistors mounted on the test board. After aging, these components could operate out of specification and thus, mask or even inject faults on the processor operation. Having this issue in mind, we replaced all passive components on board after every burn-in session, before monitoring processor operation under EMI noise injection. Note that passive components were necessary because during burn-in the component was powered on with nominal V_{DD} (3.3 V) and executed the benchmark *Dhrystone* in loop mode at a clock frequency of 70 MHz.

4. Experimental results

Since it was not observed processor performance degradation on the execution of the *Dhrystone V2.1a* benchmark up to 456 h of burn-in, we assume that degradation of this parameter was negligible. Therefore, the remaining of this paper will address results only in terms of current consumption and susceptibility to conducted EMI noise on power supply lines of the processor.

4.1. Current consumption

We observed a small increase (2.36% in average) in the current consumption of the processor. In more detail, the current increased by 2.03% for the CPU running at 100 MHz, 2.32% for the CPU at 70 MHz, 2.25% for the CPU at 35 MHz, and 2,44% for the CPU running at 10 MHz. Fig. 3 and Table 1 summarize the current consumption *versus* burn-in history.

Table 1
Final current consumption increase after 456-hour burn-in.

Processor operating frequency (MHz)	Increase of current consumption (%)
100	2.03
70	2.32
35	2.25
10	2.44
Average:	2.36

4.2. Susceptibility to conducted EMI (voltage dips)

By definition, a fault is said to be detected if: (a) the processor crashes (*i.e.*, the component stops functioning and needed power cycling to resume normal operation), or (b) the processor yields an erroneous output while executing the *Dhrystone* algorithm. The processor executed the *Dhrystone* algorithm and at specific checkpoints, it sent partial results to the Test Host Computer (THC) through an optical fiber link (serial port). After reading the incoming data sent by the processor, the THC compared them against golden values previously computed and stored in memory. If the comparison operation failed, the THC signaled a failure.

As a figure of merit, approximately 80% of the observed faults were from type (a): the processor crashed while exposed to conducted EMI noise and needed power cycling to resume normal operation. The remaining 20% of the faults were from type (b): the processor issued an incorrect output while executing the *Dhrystone* algorithm, which was detected by the THC. In the latter case, one of the two possibilities occurred: (p_1) after issuing the incorrect output, the processor executed the code until the end and was power cycled by the watchdog before restarting another *Dhrystone* run, or (p_2) after issuing the incorrect output, the processor was lost in the *Dhrystone* execution and after a given time period it was power cycled by the watchdog to restart another *Dhrystone* run.

To guarantee that the processor started executing the *Dhrystone* code from a well-known and fault-free condition during noise injection, the on-chip watchdog was adjusted to reset the processor at the beginning of every *Dhrystone* code execution, in an endless loop. Considering that the *Dhrystone* code executed in the order of 2 milliseconds and that one noise injection round had duration of 30s, the *Dhrystone* was executed in average 15,000 times at every round.

Figs. 4 and 5 were constructed with measurement results from 72 noise injection rounds (24 rounds for 0.01 ms duration, 24 rounds for 0.1 ms and 24 rounds for 1 s). For instance, we observed the occurrence of 2 faults for the fresh processor running at 100 MHz under 0.01 s voltage dips duration (Fig. 4). These 2 faults were observed during a
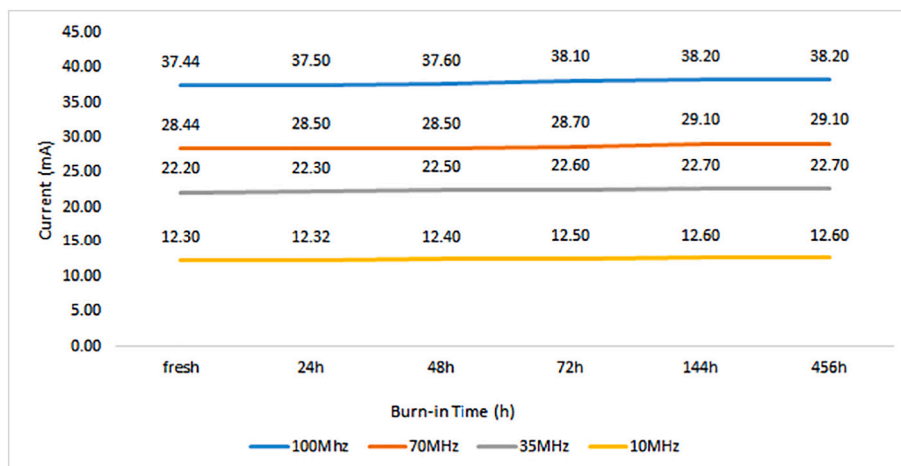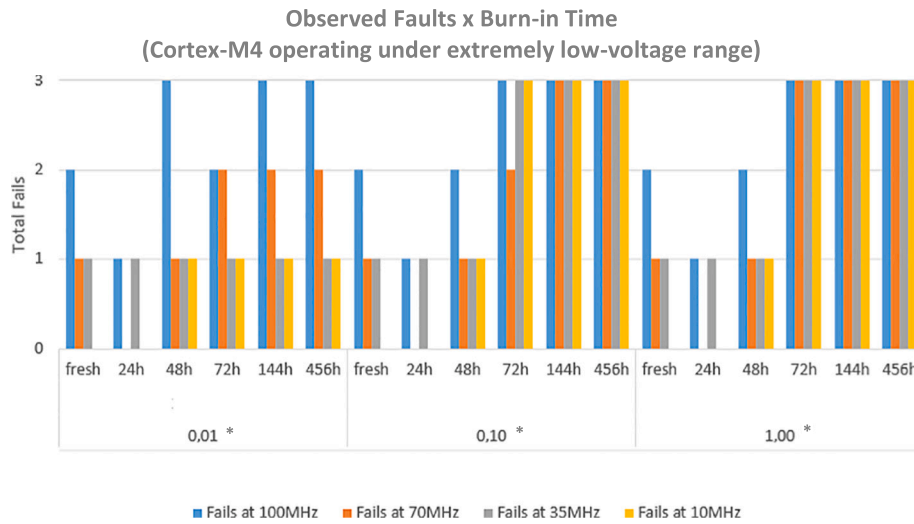

Fig. 3. Current consumption *versus* burn-in duration.

Observed Faults x Burn-in Time
(Cortex-M4 operating under extremely low-voltage range)

*Voltage-dip duration (s)

Fig. 4. Total number of failures *versus* burn-in time for voltage dips in range R1 [2.0–1.92] volts.

noise injection round of 30s. Considering that voltage dips were applied to the component at a time interval of 5 s, with a pulse duration of 0.01 s, 0.1 s and 1 s (see Fig. 2) and that one noise injection round had duration of 30s, there was in average 6 voltage dips applied to the processor input power port at every noise injection round. Thus, 432 voltage dips were applied to construct Fig. 4 (resp. Fig. 5).

4.3. Critical amplitude range R1

Fig. 4 summarizes results for the experiment we performed for voltage dips with critical amplitude range R1, whereas Tables 2 to 7 contain data we mined from Fig. 4.

4.4. Nominal amplitude range R2:

Fig. 5 summarizes results for the experiment we performed for voltage dips with nominal amplitude range R2, whereas Tables 8 to 13 contain data we mined from Fig. 5.

Table 2

Faults observed for **R1** voltage dip range with all durations, for fresh and 456-hour burn-in component.
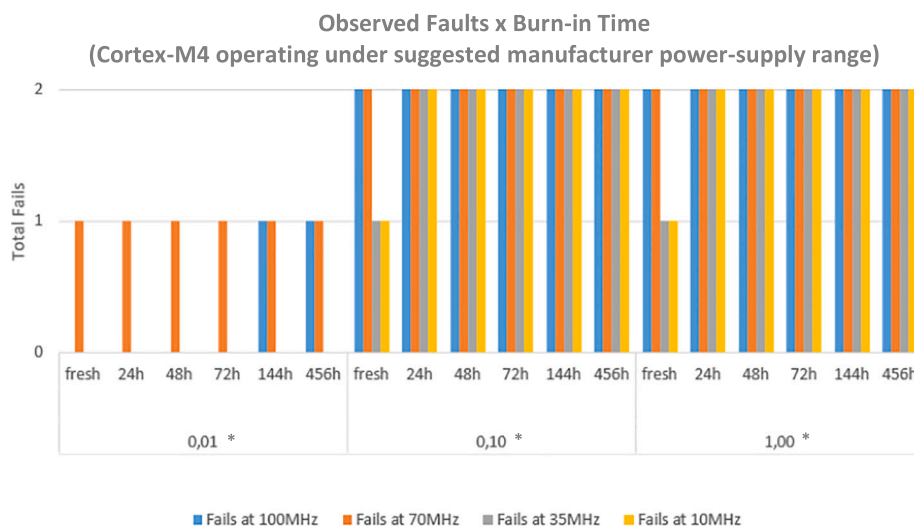
Frequency (MHz)	Fresh	456-hour Burn-in	Increase after burn-in with respect to fresh (%)
100	6	9	50
70	3	8	166
35	3	7	133
10	0	7	700
Total:	12	31	158

4.5. Conclusions

In the sequence, we tailored conclusions based on Tables 2 to 13.
Upon analyzing Tables 2 and 8, we can write the following conclusions:

Conclusion #1: 456-hour burn-in increased processor sensitivity to voltage dips with respect to the fresh component as follows:

Observed Faults x Burn-in Time
(Cortex-M4 operating under suggested manufacturer power-supply range)

*Voltage-dip duration (s)

Fig. 5. Total number of failures *versus* burn-in time for voltage dips in range R2 [3.3–2.0] volts.

Table 3
Faults observed for **R1** voltage dip range with all durations and all levels of aging, as function of clock frequency.

Frequency (MHz)	Faults
100	42
70	29
35	30
10	24
Total:	125

Table 4
Faults observed for **R1** voltage dip range with **1 s duration**, for fresh and 456-hour burn-in component.

Frequency (MHz)	Fresh	456-hour Burn-in	Increase after burn-in with respect to fresh (%)
100	2	3	50
70	1	3	200
35	1	3	200
10	0	3	300
Sub-Total:	4	12	200
Total:	16		

Table 5
Faults observed for **R1** voltage dip range with **0.1 s duration**, for fresh and 456-hour burn-in component.

Frequency (MHz)	Fresh	456-hour Burn-in	Increase after burn-in with respect to fresh (%)
100	2	3	50
70	1	3	200
35	1	3	200
10	0	3	300
Sub-Total:	4	12	200
Total:	16		

Table 6
Faults observed for **R1** voltage dip range with **0.01 s duration**, for fresh and 456-hour burn-in component.

Frequency (MHz)	Fresh	456-hour Burn-in	Increase after burn-in with respect to fresh (%)
100	2	3	50
70	1	2	100
35	1	1	000
10	0	1	100
Sub-Total:	4	7	75
Total:	11		

Table 7
Faults observed for **R1** voltage dip range, all levels of aging and clock frequencies, as function of voltage dip duration.

Voltage dip duration (s)	Faults
1	47
0.1	46
0.01	32
Total:	125

Table 8
Faults observed for **R2** voltage dip range with all durations, for fresh and 456-hour burn-in component.

Frequency (MHz)	Fresh	456-hour Burn-in	Increase after burn-in with respect to fresh (%)
100	4	5	25
70	5	5	0
35	2	4	100
10	2	4	100
Total:	13	18	38

Table 9
Faults observed for **R2** voltage dip range with all durations and all levels of aging, as function of clock frequency.

Frequency (MHz)	Faults
100	26
70	30
35	22
10	22
Total:	100

Table 10
Faults observed for **R2** voltage dip range with **1 s duration**, for fresh and 456-hour burn-in component.

Frequency (MHz)	Fresh	456-hour Burn-in	Increase after burn-in with respect to fresh (%)
100	2	2	0
70	2	2	0
35	1	2	100
10	1	2	100
Sub-Total:	6	8	33
Total:	14		

Table 11
Faults observed for **R2** voltage dip range wth **0.1 s duration**, for fresh and 456-hour burn-in component.

Frequency (MHz)	Fresh	456-hour Burn-in	Increase after burn-in with respect to fresh (%)
100	2	2	0
70	2	2	0
35	1	2	100
10	1	2	100
Sub-Total:	6	8	33
Total:	14		

Table 12
Faults observed for **R2** voltage dip range with **0.01 s duration**, for fresh and 456-hour burn-in component.

Frequency (MHz)	Fresh	456-hour Burn-in	Increase after burn-in with respect to fresh (%)
100	0	1	100
70	1	1	0
35	0	0	0
10	0	0	0
Sub-Total:	1	2	100
Total	3		

- 2.58 times (158% increase) for R1;
- 1.38 times (38% increase) for R2.
Conclusion #2: For the fresh component, it is clear that the higher is clock frequency, the lower is processor immunity to voltage dips.
Conclusion #3: For the aged component, immunity to voltage deeps

degrades more dramatically than for the fresh one, since no matter the component is operating at low or high frequency, the observed number of faults is always higher than the one observed for the fresh at the respective operating frequency.

Table 13
Faults observed for **R2** voltage dip range, all levels of aging and clock frequencies, as function of voltage dip duration.

Voltage dip duration (s)	Faults
1	46
0.1	46
0.01	8
Total:	100

Tables 3 and 9 reinforces *Conclusions #2* and *#3*. For instance for Table 3, the component immunity degrades by 75% when we compare the number of observed faults for the processor operating at 10 MHz (24) and 100 MHz (42). For Table 9, this degradation is smaller: 18%.

From Tables 4, 5, 10 and 11 we extract the following conclusions:

Conclusion #4: 456-hour burn-in increased processor sensitivity to voltage dips with durations 1 s or 0.1 s by 3 times (200% increase) for R1 and by 33% for R2.

Conclusion #5: It seems that for the case of R1 (resp. R2) and voltage dips with durations of 1 s or 0.1 s, the clock frequency increase *does not* affect the aged processor immunity, since the number of observed faults remained constant during the whole experiment: 3 (resp.2).

From Tables 6 and 12 we extract the following conclusions:

Conclusion #6: 456-hour burn-in increased processor sensitivity to voltage dips with 0.01 s duration by 1.75 times (75% increase) for R1 and doubled (100%) for R2.

Conclusion #7: For R1, contrarily to the cases of voltage dips with durations of 1 s and 0.1 s (Tables 4 and 5), the 0.01 s duration affects the aged processor immunity as long as frequency increases from 10 MHz (1 fault) to 100 MHz (3 faults). In this case the number of observed faults triplicated, while in Tables 4 and 5 the number of faults remained constant and equal to 3. Similar reasoning is valid for R2, since we observe the occurrence of faults above 70 MHz, as seen in Table 12, while it remains constant on Tables 10 and 11.

From Tables 2, 3, 8 and 9 we extract the following conclusion:

Conclusion #8: voltage dips inside the critical amplitude range R1 (2.0 V down to 1.92 V) are more harmful to the processor than those in the nominal voltage range recommended by the manufacturer (3.3 V down to 2.0 V). As seen in Tables 2 and 3 (R1), we observed a total of 43 and 125 faults, respectively, whereas for Tables 8 and 9 (R2), we counted 31 and 100 faults, respectively.

From Tables 4–6, 10–12 we extract the following conclusion:

Conclusion #9: Voltage dips with longer durations (1 s and 0.1 s) are *more harmful* to the processor immunity than shorter dip durations (0.01 s). As observed for R1 in Tables 4–6, we counted 16, 16 and 11 faults, respectively. For R2 in Tables 10–12, we counted 14, 14 and 3 faults, respectively.

Tables 7 and 13 also confirm *Conclusion #9*. On Table 7, for 1 s duration voltage dips we observed 47 faults against 32 for 0.01 s duration voltage dips (*i.e.* an increase of 47%). On Table 13, this difference is even larger: for 1 s duration voltage dips we observed 46 faults against 8 for 0.01 s duration voltage dips (an increase of 475%).

5. Discussions

In the light of the aforementioned results, this sub-section deals with answering a few questions and tailors some conclusions.

Question #1: How can we explain the link between aging and conducted EMI susceptibility level for the tested COTS processor?

Answer: aging affects the circuit by slowing down signal propagation along with the logic and thus, eroding the time slack allocated for the clock signal as defined by design [18–20]. If the time slack becomes too small, and if the circuit critical paths are exercised, we may observe transient faults during circuit operation. Ultimately, for high aging levels, when the time slack becomes negative for the exercised critical paths, one could expect permanent IC failure. In the specific case of our experiment, the Cortex-M4 processor was exercised with the *Dhrystone V2.1a* benchmark [16]. This is a well-known application from the designers' community used since the 80's to exercise the entire set of mathematical (integer) instructions and data string manipulations of processors. So, a good software candidate to exercise critical paths of the Cortex-M4 logic.

At the same time, conducted EMI noise on power supply lines also produces the similar effect, by slowing down signal propagation thought the logic, which in turns, increases the probability of desynchronization between the signal propagation and clock triggering, and so the occurrence of transient faults in the circuit [21,22].

It should be noticed that we did not observe permanent or transient faults for the processor aged up to 456 h, when operating at nominal conditions (V_{DD} = 3.3 V, clock frequency = 100 MHz). So we assume that aging up to this point was not large enough to shrink time slack in such a way to provoke these types of faults on the processor while running at nominal conditions.

However, in the presence of conducted EMI noise on power supply pins, we observed that the 456-hour aged processor presented a larger number of faults when comparted to its fresh version. This observation leads us to conclude that when aging is combined with conducted EMI noise on input power pins the consequences are more harmful to the Cortex-M4 processor than their separate effects.

Question #2: Why are voltage dips with longer durations more harmful than shorter ones?

It is our understanding that long-duration voltage dips corroborate to discharge circuit internal nodes' capacitance to lower levels than those levels induced by short-duration voltage dips. In other words, as shorter is the voltage dip, closer is the voltage at the circuit internal nodes to their nominal values generated during fault-free operation. Table 7 (for range R1) and Table 13 (R2) support this reasoning.

Question #3: Why does the processor (either fresh or aged) present lower immunity to voltage dips at high frequencies than at low ones?

Note that the higher is clock frequency, the shorter is the time slack allocated for the clock period to accommodate signal propagation trough the logic, as defined by design. Thus, one could expect that the processor would present higher immunity to voltage dips at lower clock rates than at higher ones. Tables 3 and 9 support this reasoning.

Question #4: Why does the processor (either fresh or aged) present lower immunity to voltage dips at range R1 than R2?

Note that as defined by the manufacturer, the recommended component minimum and maximum operating voltages are 2.0 and 3.3 V, respectively. On the other hand, we experimentally measured the minimum operating voltage for this component as 1.92 V. This scenario suggests that range R1 ([2.0–1.92] volts) is more harmful to the processor immunity than R2 ([3.3–2.0] volts) since R1 is extremely low voltage and is outside the manufacturer's recommended operation, while R2 is not.

6. Conclusions of the Work

We have analyzed the conducted EM immunity sensitivity of one of the most used processors for consumer applications, the ARM Cortex-M4 processor, with respect to aging. In this work, we based measurements for conducted EMI on the IEC 61000–4-29 std., whereas component aging was guided by the MIL-STD-833H Part 1015.9.

We *did not* observe faults for the fresh or aged processor up to 456 h of burn-in, when it is operating at nominal conditions (V_{DD} = 3.3 V, clock frequency = 100 MHz, *i.e.*, no noise applied). However, we observed that the fresh processor presented 25 faults when operating in EMI noise environment (resp. 49 faults after 456-hour burn-in). This yields 96% EMI noise immunity degradation after aging, considering that in the experiment the processor was exposed to voltage dips at extremely low voltage range (R1: [2.0–1.92] volts) and nominal voltage range as recommended by the manufacturer (R2: [3.3–2.0] volts). If we analyze immunity degradation separately for R1 or R2, then after burn-in the processor EMI noise immunity degraded by 158% for voltage dips produced inside range R1 and 38% for R2, with respect to the fresh processor.

Having analyzed these numbers, it is our understanding that when aging is combined with conducted EMI noise on input power pins, the consequences are more harmful to the Cortex-M4 processor than their separate effects.

Moreover, we observed *no* performance degradation on the execution of the *Dhrystone V2.1a* benchmark after 456-hour burn-in procedure. This is a well-known application from the designers' community used since the 80's to exercise the entire set of mathematical (integer) instructions and data string manipulations of processors.

We measured a small (2.36%) increase in processor current consumption after 456 h of burn-in at 125 °C. This increase is probably due to some physical degradation. However, it is our understanding that this degradation was not enough to affect processor's performance to a noticeable level.

We performed the experiment based on one single component. This fact does not affect negatively the work scientific findings and conclusions, since all measurements have been made to compare two versions of the same component: a fresh and an aged version, surrounded by always-fresh passive components, and guided by specific standard procedure. Nevertheless, for future work, we intend to analyze if additional samples from different fabrication lots can affect (and if so, in which extent) the obtained results. We understand that a statistical study would also provide an important contribution to this work.

We also intend to overclock the fresh and aged versions of the processor while executing the *Dhrystone* benchmark. This will help us to understand the extent of the physical degradation, despite the fact that it was not observed performance penalty.

CRediT authorship contribution statement

Juliano Benfica: Methodology, Formal analysis, Investigation. **Fabian Vargas:** Supervision, Conceptualization, Methodology, Formal analysis, Investigation. **Matheus Fay Soares:** Software, Resources, Data curation. **Dorian Schramm:** Software, Resources, Data curation.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.microrel.2020.113884.

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