Analysis and detection of hard-to-detect full open defects in FinFET based SRAM cells

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***Abstract*—FinFET technology is used in leading high-performance/power-efficient electronic products. This technology has proven its efficiency after 22nm technology nodes. However, FinFET technology has new manufacturing and design complexities. Thus, it is required to study the behavior of defects in FunFET-based SRAM memories, and developing new test strategies for those defects that are not covered by conventional test strategies based on CMOS fault modeling. This paper is oriented to open-gate defects hard-to-detect that are unique to FinFET based SRAM memory cells. The open-gate defect affects only one of the parallel fins of the driver transistors of the memory cell. The behavior of these defects is studied for the hold, read and write operations using realistic defect models. By using a shorter write time test, the detection of these defects is investigated. The effectiveness of the shorter write time test method at nominal parameters and under process variations is evaluated. The detection probability of these defects can be further enhanced using a higher power supply voltage.**

I. Introduction

The continuous scaling in CMOS technology has allowed the development of electronic products with better performances and lower power consumption [1]. However, scaled CMOS technologies are severely constrained by short-channel effects (SCEs) and process variations (PVs) due to random dopant fluctuations (RDFs). After 22 nm node, FinFET technology has allowed further scaling of the semiconductor technology. In FinFET devices, the gate wraps around a thin slice of silicon, which is known as the fin. The inversion channel is created at the three walls of the fin. The wrapping of the fin results in a stronger electrostatic control over the transistor channel and hence improving SCE behavior [2].

New defects may occur in FinFET circuits as new technologies are incorporated for their manufacturing, and the use of complex multi-fin/multi-finger structures. Fault modeling in FinFET based-circuits has been addressed by some authors [3] [4]. Conventional CMOS fault models can cover some defects, but some defects are specific to FinFET technology. The authors have found that open defects in multi-fin/multi-finger structures exhibit small delays increase, which is difficult to be detected. FinFET based SRAM cells built at highly reduced geometries with complex manufacturing process are susceptible to manufacturing defects. Some research studies on the test of FinFET-based memories have being conducted. Harutyunyan et al. [5] [6] have investigated the detection of manufacturing defects such as opens and shorts in FinFET memory cells. Several new fault types that are specific to FinFETs are identified. The impact of parameter variations on the fault coverage of FinFET memory cells when dealing with FinFET-specific faults are studied in [7]. Chen at al. [8] have studied FinFET specific faults in a FinFET-based SRAM circuit. They have found that some dynamic faults are hard-to-detect. The authors propose a BIST scheme to detect these hard-to-detect faults. The proposed BIST scheme is based on capturing the delay in the BL discharging phase using a bit line delay sensor circuit.

In this paper, the behavior of hard-to-detect full open defects in FinFET memory cells is studied. In this paper, realistic locations of the defect are considered from a layout extraction taking into account the parasitic capacitance due to MOL layers. Butterfly curves for static operation and dynamic behavior are analyzed. By using a shorter write time test, the detection of these defects is investigated. The effectiveness of the shorter write test method at nominal parameters and under process variations is evaluated.

The rest of this paper is organized as follows. In Section II, the classical modeling of open gate defects in planar CMOS is illustrated, In Section III, the behavior of the defective cell is analyzed. In Section IV, the detection of hard-to-detect full open defect in the FinFET memory cell is investigated. In Section V, the effectiveness of the shorter write test is evaluated at nominal parameters and under process variations. In Section VI, the detection of these defects is enhanced by using a higher power supply voltage. Finally, Section VII presents the conclusions of this work.

II. Modeling of open-gate defects in planar CMOS

Figure 1 shows the traditional defect model for a single open-gate defect. The induced voltage at the floating node (V_{if}) for a single nMOS open can be estimated by [9],

$$V_{if} = \frac{C_{gd,n}}{C_T} V_o + \frac{-Q_{GT}}{C_T} + V_{f_{ini}} \quad (1)$$

where Q_{GT} is the intrinsic gate charge, and C_T is the sum of all capacitances tied to the floating gate. $V_{f_{ini}}$ is an initial voltage at the floating node that depends on the trapped gate charge. As the value of this charge can not be predicted, the behavior of a logic cell is analyzed for an assumed range of possible initial voltages at the floating node. In this work, a

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range between -0.2V and 0.2V of initial voltages is assumed. Nevertheless, the trends of the results remain for other values of the trapped gate charge.

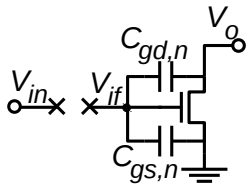
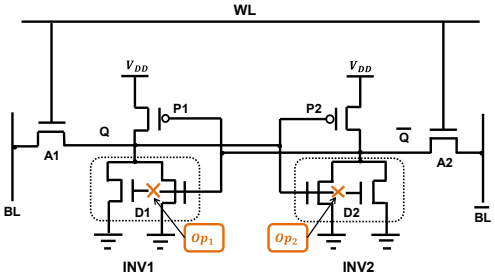


Fig. 1: Modeling of a single open-gate defect.

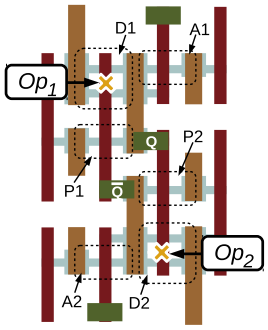
For single open-gate defects inside a cell, the influence of coupling signals at higher metal levels can be neglected [9].

III. Behavior of the Defective Cell

Fig. 2 shows a schematic and layout of a SRAM cell implemented with FinFETs [10]–[13]. The number of fins in the implemented SRAM cell is 2, 1, 1 and for the pull-down (driver), the pass gates (access) and the pull-up transistors. The marks placed in both the schematic and the layout (See Fig. 2) show the location of an open-gate defect analyzed in this work. This open affects only one of the parallel fins of the driver (pull-down) transistor of the memory cell. As there exists a non-defective fin, the memory cell works correctly for a broad spectrum of conditions. Hence, this open-gate defect is hard to be detected by conventional test methodologies.



(a) Circuit schematic of the SRAM cell



(b) Layout

Fig. 2: FinFET SRAM cell and open locations

A Raphael Field Solver is used to obtain an accurate extraction of the fringing capacitances (Middle-Of-Line -MOL- interconnects) of the memory cell with and without open-gate defects. The simulated 3D structures were based on FinFET process technology [14]. SiN was used as a dielectric with a relative permittivity of 7.5. A Spice library was created with the results of the extraction, and the simulation model was the 14nm PTM-MG bulk model [15]. The power supply (V_{DD}) was set-up to 0.8V using a transient waveform at Spice. All the peripheral circuits for the write and read operations have been included.
Next, the behavior of the defect-free cell is analyzed for the following operations: a) hold, b) read, and c) write. Possible values of trapped gate charge are considered using different initial voltages at the floating node ($V_{f_{ini}}$).

From now on, the analysis is focused in open Op_1 (See Fig. 2). As the memory cell is symmetrical, this analysis is also valid for the other possible open-gate defect Op_2.

1) Hold Operation: The access transistors are turned off, and the nodes Q and $\overline{Q}$ are forced to desired states for different initial voltages conditions at the floating node. Then, the cell is released and naturally evolves to its final state. Butterfly curves (See Fig. 3) have been obtained for the Hold Operation. They present two stable points with well-defined noise margins, which means that the cell is capable of holding both logic states. The voltages at Q and $\overline{Q}$ present minimal deviations from their desired voltage values.

For 1-hold at Q, the defective transistor may be in on-state but its strength is not enough to cause a bit-flip. For 0-hold at Q, the second driver transistor of the cell is non-defective, and the memory cell is capable of holding a 0 at node Q.

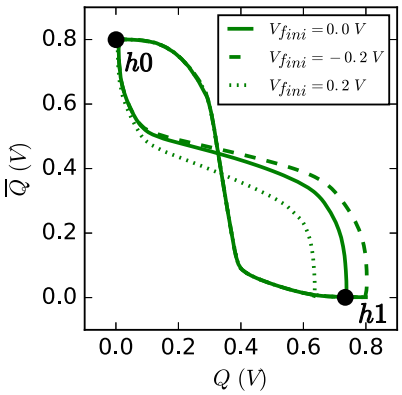
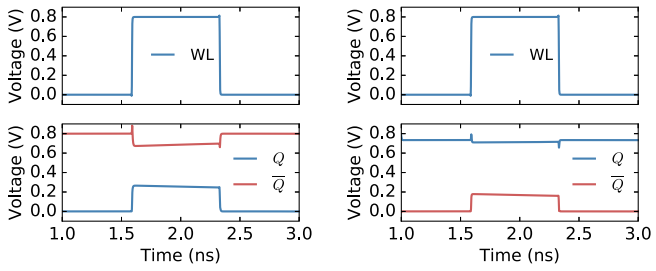


Fig. 3: SNM behavior of the SRAM cell in Hold operation, Op_1 in Fig 2.

2) Read Operation: The behavior of the memory cell for a read operation is analyzed. Open Op_1 (See Fig. 2) may affect a 0-read operation as the driver transistor of the memory cell is responsible for making a small discharge of the pre-charged line BL. Then, the sense amplifier compares between BL and $\overline{BL}$ and gives the read value to the output. For 0-read (See Fig. 4a), when WL goes 1 the driver transistor of the inverter INV1 is responsible for making a small discharge of the pre-charged voltage at BL. This capability is decreased because one of the parallel fins of the driver transistor is defective. However, the memory cell is correctly read as the transient simulation shows. A similar behavior is observed for

different conditions of initial voltages at the floating node. Some bad readings and bit-flip of the memory cell may occur when process variations are considered. The impact of process variations will be analyzed later.

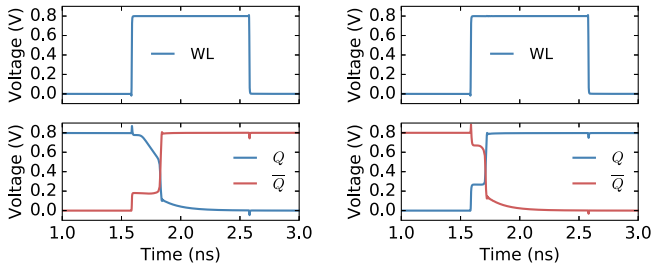
For 1-read (See Fig. 4b), when WL goes 1 the driver transistor of the inverter INV2 is responsible for making a small discharge of the pre-charged voltage at BL. Because both parallel fins of the driver transistor of INV2 are defect-free, the cell is correctly read as the transient simulation shows.



(a) Read-0 (b) Read-1

Fig. 4: Read operation for a defective SRAM cell, Op_1 in Fig 2.

3) Write Operation: Fig. 5 shows the transient behavior of the Write Operation of a defective SRAM cell. It can be observed that the cell is able to write both logic states (0-write and 1-write) when WL goes 1. A similar behavior is observed for different values of initialized voltages at the floating node.



(a) Write-0 (b) Write-1

Fig. 5: Write operation of defective SRAM cell, Op_1 in Fig 2.

The previous analysis shows that the defective cell behaves correctly for the operation modes of the memory cell at different conditions of the trapped-gate charge at the floating node. These characteristics make this open-gate defect hard to be detected.

IV. Detection of Hard-to-Detect Full Open Defects

Fig. 6 shows the static voltage transfer curves (SVTC) for the defect-free (at the top in Fig. 6) and defective (at the bottom in Fig. 6) SRAM cell shown in Fig. 2a. Open-gate defect Op_1 at one of the parallel fins of the driver transistor ($D1$) of inverter INV1 (See Fig. 2a) is considered. Defect-free and defective static voltage transfer curves for the inverter INV1 are illustrated in Fig. 6. The defect-free SVTC of inverter INV2 is also shown.

The SVTC of inverter INV1 for the defective case shifts to the right (See at the bottom in Fig. 6) as its nMOS network loss drive strength due to the open-gate defect. Let us assume a 0-logic (1-logic) initial state at node Q ($\overline{Q}$). Then, a 1-write operation is made. Node Q goes up and node $\overline{Q}$ is pulled-down. As the SVTC of the defective cell has moved to the right, a smaller voltage drop at node $\overline{Q}$ (ΔV_{def}) is required to reach the threshold voltage of the defective inverter INV1 to start regenerative feedback (See Fig. 6). On the other hand, for the defect-free cell, a larger voltage drop at node $\overline{Q}$ ($\Delta V_{def-free}$) is required to reach the threshold voltage of the defect-free inverter INV1 to start regenerative feedback (See Fig. 6).

Based on the previous observations, a shorter write time time [16] can be used to detect the hard-to-detect full open defects. At test mode, a 1-write operation with a shorter write time is applied to test open-gate defect Op_1 (See Fig. 6). The memory cell behaves as follows:

- **Bad write of the defect-free cell**.- For the defect-free cell, the voltage at node $\overline{Q}$ does not fall enough to start regenerative action due to the shorter write time. Hence, the cell is bad written.
- **Good write of the defective cell**.- For the defective cell, the lowered voltage at node $\overline{Q}$ can initiate regenerative feedback as the static transfer curve of the defective inverter is moved to the right. Hence, the cell is good written.

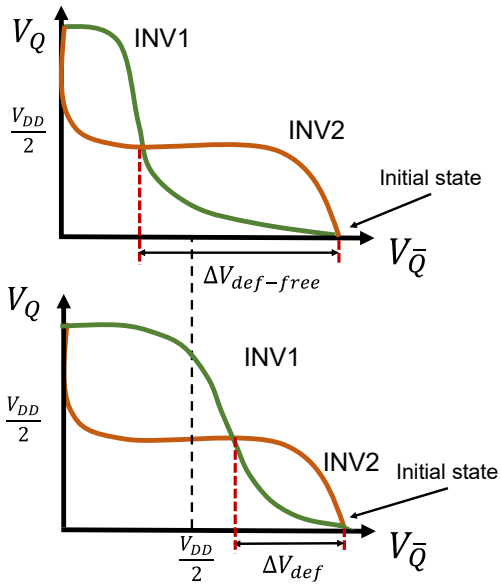
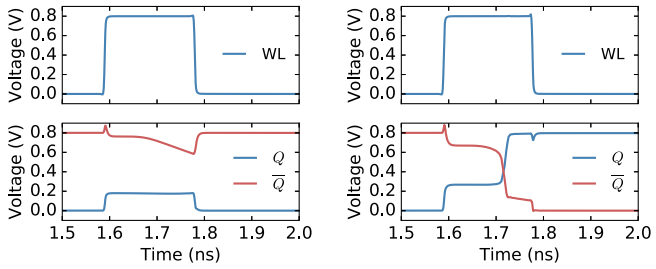


Fig. 6: Static voltage transfer curves for the defect-free and defective SRAM cell.

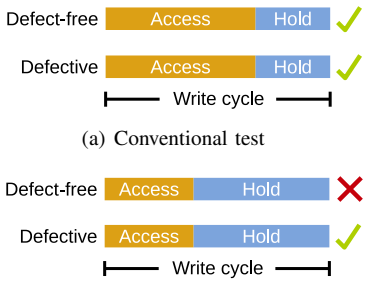
Fig. 7 illustrates a transient simulation with the shorter write time test. It can be observed that the defect-free cell is bad written, and the defective cell is good written.



(a) Defect-free (b) Defective

Fig. 7: Behavior of the defect-free and defective SRAM cells with a shorter write time.

The write operation of a SRAM cell can be divided into two regions (See Fig. 8). The first region is when the access transistors are ON (access region) to write the cell. The second region is when the access transistors are OFF (hold region). A defective SRAM cell is written faster than a defect-free cell; therefore, both the defect-free and defective cells will be successfully written at a conventional test (See Fig. 8a). For a shorter write time (See Fig. 8b), the defect-free cell will be unable to write the desired bit. However, the defective cell will be written successfully, and hence, the defect can be detected.



(a) Conventional test

(b) Shorter-write test

Fig. 8: Conventional test and shorter-write test.

Unlike conventional test, this technique is based on the fact that a defect-free cell fails the write operation, but a defective cell is able to perform correctly the write operation.

V. Application of the Shorter Write Time Test

A. Shorter-write time test at Nominal Parameters

Fig. 9 shows the fault coverage of open-gate $Op1$ using a conventional test and shorter write time test. For a conventional test three operations are made: a) Write 0-logic (1-logic), b) Write1-logic (0-logic), and c) Read 1-logic (0-logic). A write time slightly larger than the required *minimum write time* [1] is used. Initial voltages between -0.2V and +0.2V at the floating node have been considered for the trapped gate charge. It can be observed that the open is detected using the shorter write time test when nominal parameters for the SRAM cell are considered.

[1]Minimum write time is defined as the minimum required time to write both logic states correctly at the memory cell.

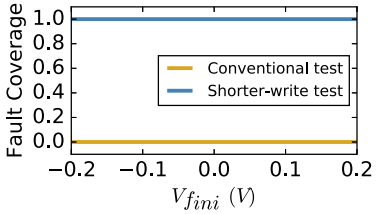


Fig. 9: Fault coverage of defective SRAM cell, Op_1 in Fig 2.

B. Shorter-write test under process variations

The effectiveness of the shorter write time test has been evaluated under process variations in the SRAM memory cell. Local and global process variations are considered [17], [18]. Table I shows the local (σ_L) and global (σ_G) standard deviations for the parameters T_{fin} and L_g, and only local standard deviation for the parameter Φ_M.

According to the ITRS, the expected 3σ value of line width variations for the 14nm node is 1.4 nm [19]. The assumed 3σ value due to global variations is 10% of the nominal parameter value [17], [18].

TABLE I: Process parameters variation [17]–[21]

Parameter	Local variations	Global variations
Φ_M	$3\sigma_{\Phi_M,L} = 90mV$	–
T_{fin}	$3\sigma_{T_{fin},L} = 1.4nm$	$3\sigma_{T_{fin},G} = 0.8nm$
L_g	$3\sigma_{L_g,L} = 1.4nm$	$3\sigma_{L_g,G} = 1.4nm$

The *minimum write time* of a defect-free memory cell may take different values due to process variation of the parameters. Assuming that the parameters fluctuate following a Gaussian distribution, the *minimum write time* also follows a Gaussian distribution as shown in Fig. 10. Two distinct regions appear: a) Assured good write, and b) Assured bad write. Good write under process variations is assured when the write time is at least $(\mu + 3\sigma)_{def-free}$ (See Fig. 10), and bad write under process variations is assured when the write time is non-greater than $(\mu - 3\sigma)_{def-free}$ (See Fig. 10).

The *minimum write time* distribution of a defective memory cell shifts to the left with respect to the defect-free distribution, but the two distinct "assured" regions also appear similarly to the defect-free cell. In this case, $(\mu + 3\sigma)_{def}$ and $(\mu - 3\sigma)_{def}$ corresponds to the defective distribution.

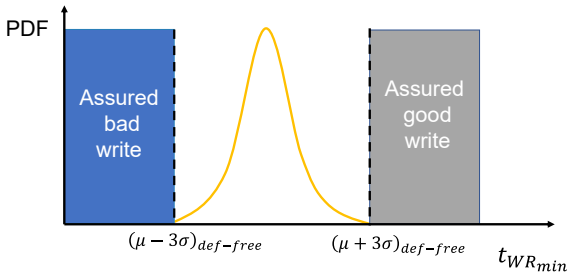


Fig. 10: Minimum write time distribution for a defect-free memory cell.

Let us define the test conditions to apply the shorter write time test. As previously stated, the shorter write time test technique is based on bad write of a defect-free cell and good write of a defective cell when a shorter write time is applied. The following two conditions need to be satisfied at test mode:

1) *Condition 1*.- Bad write of the defect-free cell must be assured under process variations. This is achieved by choosing a write time lower than $(\mu_D - 3\sigma_D)_{def-free}$ of the *minimum write time* distribution of the defect-free cell (See Fig. 10). This condition ensures no yield loss.
2) *Condition 2*.- Good write of the defective cell must be assured under process variation. This is achieved by choosing a write time greater than $(\mu + 3\sigma)_{def}$ of the *minimum write time* distribution of the defective cell. This condition maximizes detection of the open-gate defect.

Fig. 11 shows possible *minimum write time* distributions for the defect-free and defective cells when the distributions do not overlap. In this case, both *Condition 1* and condition *Condition 2* can be satisfied (See Fig. 11). The write time (t_{WR}) at test mode is chosen at $(\mu_D - 3\sigma_D)_{def-free}$ (See Fig. 11). At this point where the two curves do not overlap both conditions are satisfied. For non-overlapped distributions, the open-gate defect is detected under any process condition of the parameters..

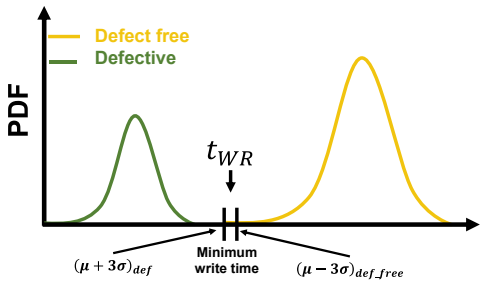


Fig. 11: Computing detection probability for non-overlapping minimum write time distributions.

Fig. 12 shows possible *minimum write time* distributions for the defect-free and defective cells when the distributions overlap. In this case, *Condition 1* can be assured, but *Condition 2* can not be fully assured. The write time (t_{WR}) is chosen at $(\mu - 3\sigma)_{def-free}$ of the *minimum write time* distribution of the defect-free cell to maximize defect detection. Because overlapping of the distribution curves, 100% fault coverage of the open-gate defect can not be assured. The shadowed area (See Fig. 12) gives the detection probability. The detection probability of the open-gate defect is computed using equation 2 [22],

$$P = \int_{-\infty}^{t_{WR}} \frac{1}{\sqrt{2\sigma_{def}^2 \pi}} e^{-\frac{(x-\mu_{def})^2}{2\sigma_{def}^2}} dx \qquad (2)$$

where x is the write time, t_{WR} is the used time for shorter-write test, and μ_{def} and σ_{def} are the mean and standard deviation of the minimum write time distribution of the defective cell.

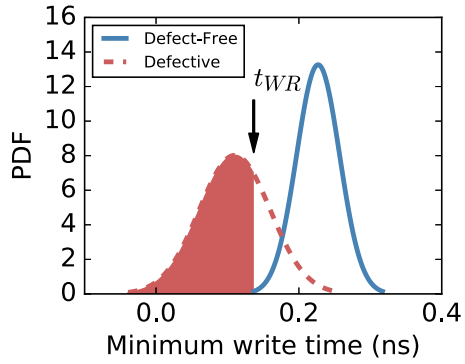


Fig. 12: Computing detection probability for overlapping minimum write time distributions.

Fig. 13 shows the detection probability of a defective SRAM cell using conventional test and the shorter write time test. The write time (t_{WR}) at test mode is chosen at $(\mu - 3\sigma)_{def-free}$ of the *minimum write time* distribution of the defect-free cell to avoid yield loss. The detection probability decreases with higher positive values of $V_{f_{ini}}$. This is because of the overlap between the PDFs of the defect-free and defective cells increases. It can be observed that the detection probability (Fault Coverage) is significantly improved using the shorter write time test in comparison to conventional test.

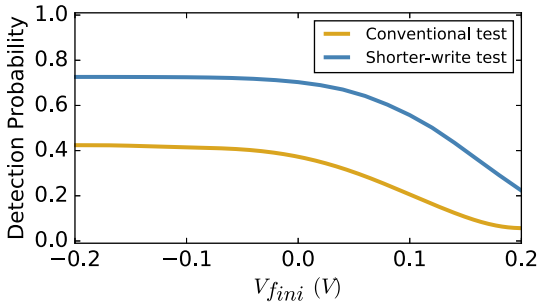


Fig. 13: Detection probability using a shorter-write test and conventional test at nominal V_{DD}, $t_{WR} = 140$ps.

Table II shows the detection probability of the shorter write time test for different write time values (t_{WR}). In the first column, it is given the percentage of reduction of the used t_{WR} with respect to the minimum write time of the defect-free memory cell to assure good write in the presence of process variations (See Fig. 12). The detection probability decreases as a lower value of t_{WR} is used. This is because of the shadowed area of the defective distribution reduces (See Fig. 12).

TABLE II: Detection probability using a shorter-write test at nominal V_{DD}

t_{WR} (%)	Detection probability		
	$V_{f_{ini}} = -0.2V$	$V_{f_{ini}} = 0V$	$V_{f_{ini}} = 0.2V$
57 %	0.73	0.70	0.22
66 %	0.51	0.47	0.05
76 %	0.28	0.25	0.00

VI. Enhanced detection probability

The detection probability of the open-gate defect using the shorter write test can be further improved using a higher power supply voltage. This allows reducing the overlap between the distributions of the defect-free and defective cells.

Fig. 14 shows the detection probability of a defective SRAM cell using a shorter-write test. The results obtained by using $V_{DD} = 0.8V$ (nominal condition) and $V_{DD} = 1V$ are shown. It can be observed that the detection probability increases with the use of a higher power supply voltage. A higher V_{DD} allows that the shorter write test achieves a better detection probability.

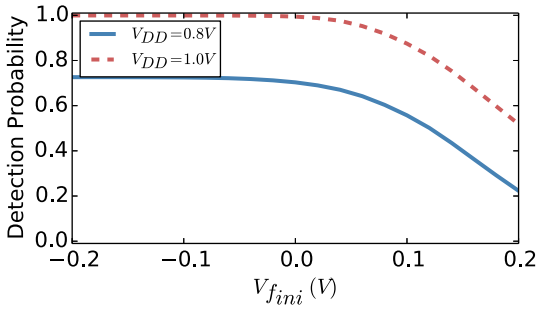


Fig. 14: Detection probability using a shorter-write test at nominal and higher power supply voltage, $t_{WR} = 140$ps@$V_{DD} = 0.8$V, $t_{WR} = 90$ps@$V_{DD} = 1$V.

Table III shows the detection probability of the proposed test methodology for different values of the write time (t_{WR}). The probability of detection improves significantly using a higher V_{DD} (See Table III) in comparison to using a nominal V_{DD} (Table II).

TABLE III: Detection probability using a shorter-write test at a higher V_{DD} ($V_{DD} = 1V$)

t_{WR} (%)	Detection probability		
	$V_{f_{ini}} = -0.2V$	$V_{f_{ini}} = 0V$	$V_{f_{ini}} = 0.2V$
46 %	1.00	0.99	0.52
58 %	0.96	0.91	0.24
70 %	0.66	0.55	0.07

VII. Conclusions

The behavior of hard-to-detect full opens unique to FinFET technology has been investigated. The open- gate defect affects only to one of the parallel fins of the driver transistors of the memory cell. The shorter write time test method significantly improves the detection probability of the defect. The detection of these defects has been investigated at nominal parameters and under process variations. Furthermore, the detection of these difficult to detect defects can be enhanced by increasing the power supply voltage. The results suggest that the shorter writ test can also be applied to other defects decreasing the driving capability of any one of the driver transistors of the memory cell.

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