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Combined ionizing radiation & electromagnetic interference test procedure to achieve reliable integrated circuits

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ABSTRACT

International standards have been proposed and used to test Integrated Circuits (ICs) for Total-Ionizing Dose (TID) and Single-Event Upset (SEU) as well as for Electromagnetic Interference (EMI). Nevertheless, these standards are separately applied to the IC or electronic system, one after the other, and do not take into account the combined effects of these types of radiation may take over the ICs. In more detail, there is no standard that rules combined tests for TID, SEU and EMI. This paper aims to fulfill this lack of product quality information and proposes a new methodology to improve the reliability of ICs by performing combined tests for TID, SEU and EMI. We also present recent experimental results from combined measurements that we performed on a commercial FPGA IC widely used in critical embedded applications such as aerospace and automotive. Such results strongly suggest that the effects of radiation are not negligible and should be taken into account if one intends to design reliable embedded systems.

1. Introduction

Technology scaling, which made electronics accessible and affordable for almost everyone on the globe, has advanced integrated circuit (IC) and electronics performance since sixties. Nevertheless, it is well recognized that such scaling has introduced new (and major) reliability challenges to the semiconductor industry [1–5]. International standards have been proposed and used to test ICs for ionizing radiation (such as total-ionizing dose: TID [6,7] and single event upset: SEU [8,9]) as well as for electromagnetic interference (EMI) [10–12].

Notwithstanding, these standards do not take into account the combined effects of these types of radiation may take over the ICs. In more detail, there is no standard that rules combined tests for TID, SEU and EMI. Previous published works [5,13–15] suggest that the combined effect of ionizing radiation plus strong electromagnetic fields on electronics can be severe enough to justify serious concern from design engineers, in particular for critical applications where the event of a failure can be catastrophic, e.g., in automotive, transportation and aerospace. For example, for a satellite operating in a low earth orbit (LEO), assume that every time the satellite passes through the Van Allen Belts (whose passage, typically, could take a few minutes), the electronics is simultaneously exposed to (radiated or conducted) EM interference on the power supply lines. Then, one could expect that the failure rate (the average number of bit flips in memory elements of the chips operating onboard) would be increased in comparison to the same electronics exposed to the Van Allen Belts operating at nominal V_{DD} conditions. So, it is easy to suppose and accept that performing combined tests would provide the designer with better estimations for the satellite electronics reliability. This paper aims to fulfill this lack of product quality information and proposes a new methodology to improve the reliability of ICs by performing combined tests for TID, SEU and EMI. Even though there exist several other types of EMI, this is the first study addressing the problem. So, focus is given to voltage dips (IEC 61000-4-29) due to its importance as EMI source, as well as the relatively low complexity and cost to implement the test procedure and laboratory infrastructure. As future work, it is our intention to extend this study to voltage variations and short interruptions (also IEC 61000-4-29), ripple on the d.c. input power port (IEC 61000-4-17) and electrical fast transient/burst immunity on d.c. input power pins of the IC (61000-4-4) [19]. The paper is organized as follows: first, Section II2 addresses radiation background mechanisms impacting the reliability of Very Deep SubMicron (VDSM) ICs. The TID, SEU and EMI combined

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effects on the reliability of modern ICs are briefly discussed. Then, Section III3 presents the proposed methodology for combined test and the required laboratory setup. Finally, Section IV4 describes recent results from experimental combined measurements of a commercial Field Programmable Gate Array (FPGA) IC widely used for critical embedded applications such as aerospace and automotive, where electronic systems have to operate in noisy environments under high degrees of reliability to transient faults.

2. Preliminaries

2.1. Previous works dealing with combined effects

Along the history, there is only a few works trying to understand and quantify the combined effects of ionizing (total-ionizing dose: TID) and non-ionizing (EMI) radiations on ICs and embedded systems. One of the first to do so was published by James R. Marbach et al. in 1978 [16]. A few years later, Charles A. Katzenberg et al. [17] published another scientific paper in 1982. These works dealt with studying the radiation combined effects on pacemakers that were exposed to therapeutic levels of ^{60}Co radiation as well as to the electro-magnetic fields associated with betatrons and linear accelerators. The whole problem turns around the fact that when cancer patients with implanted pacers undergo radiation therapy it is important to know whether the treatment will have any deleterious effects on the pacer, thus placing the patient in jeopardy from malfunction. Malfunction may consist of continuous or intermittent spurious signals or an interruption of normal pacer signals. In this context, radiation therapy exposes a pacemaker to ionizing radiation alone (^{60}Co), or ionizing radiation plus strong electromagnetic fields (linear accelerators and betatrons), which may induce noise and interference into reactive electronic circuits. At the end of their work, Marbach and Katzenberg concluded that the combined effect of ionizing radiation plus strong electromagnetic fields on pacemaker function was severe enough to justify some concern with the patients.

Three decades later, Nicholas A. Estep et al. [13] investigated the effect of combined EMI and ionizing radiation on two complementary metal–oxide–semiconductor inverter technologies (CD4069 and SN74AUC1G04), which were analyzed for their static performance in response to both EMI and gamma radiation up to 132 krd(Si). In this study, they observed that n- and pMOS devices presented shift and distortion of the voltage and current transfer characteristics, leading to reduced noise margins and logic instability. As consequence, EMI + TID combination proved most damaging, when compared to isolated EMI and ionizing radiation experiments.

It is worth noting that none of the previous studies took into consideration the combined effects of ionizing (soft errors in memory elements) and non-ionizing (EMI) radiations on ICs. In this context, Juliano Benfica et al. [5] published a work addressing the problem of soft errors (single-event upset – SEU) and EMI. Moreover, there is an absence of a standard to rule combined tests. So far, from the best of our knowledge, there is only a draft recommendation from ITU: “Overview of particle radiation effects on telecommunications systems”, Geneva, Oct. 2016) that treats quite superficially the problem of combined effects.

In the light of the previous discussions, this paper aims to fulfill this lack of product quality information and open discussion for a new methodology to improve the reliability of ICs by performing combined tests for TID, SEU and EMI.

2.2. Background mechanisms degrading reliability

Fig. 1 presents the failure mechanisms by depicting possible threshold voltage shift curves for the n- and pMOS transistors when exposed to total ionizing dose (TID). TID effects on CMOS ICs are caused primarily by positive charge trapped in insulating layers. For

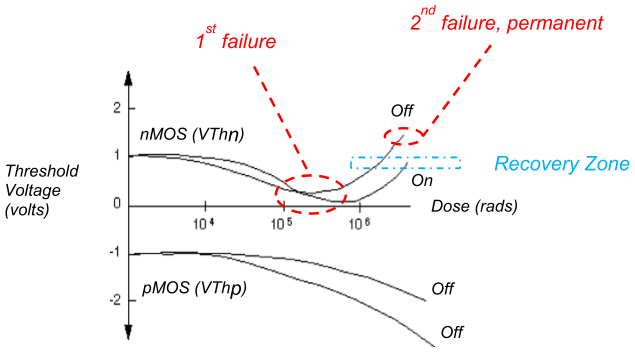


Fig. 1. Failure mechanisms for the n- and pMOS transistors: change in the V_{th} of the transistors. Adapted from Pease et al. [18].

CMOS ICs, the main TID effect is the increase of leakage currents and change in V_{th} of the devices [1,2]. For high doses, a permanent functional failure of the circuit is observed. Note that as result of TID, for nMOS transistors, the Vth_n is reduced (which may produce the 1st failures in the circuit) and then for some radiating conditions and continued TID deposition levels there is a recovery of the Vth_n driving the nMOS device back to pre-TID values (this is the *Recovery Zone*). Finally, for very high TID values, the nMOS transistor tends to cut-off and a 2nd and permanent failure of the circuit is expected. On the other hand, the pMOS transistor behavior in the presence of TID is more homogeneous, since as observed, this device always tends to cut-off as TID is being deposited.

Fig. 2 illustrates the mechanism by which a high-energy particle strike produces a single-event upset (SEU), i.e., a bit-flip in a SRAM cell. Fig. 2a depicts the moment when a high energetic particle strikes the reversed-biased depletion region of an off nMOS transistor of a SRAM cell and the immediate charge generation (Fig. 2b), whereas Fig. 2c illustrates in detail the charge collection mechanism that causes single-event upset: the instantaneous current pulse generated in the n^+p region during the collection of the charge.

Fig. 3 depicts the failure mechanism by which a conducted electromagnetic noise interferes on the integrity of the signal propagated through the IC. The increasing hostility of the electromagnetic environment caused by the widespread adoption of electronics, (mainly wireless technologies), represents a huge challenge for the reliability of real-time embedded systems. In this scenario, EMI produces Power Supply Disturbances (PSD), which in turn, if large enough, may produce transient faults inside the chip. In other words, signals outside noise margins can be erroneously interpreted and stored by memory elements (e.g., flip-flops) placed at the end of critical paths. For readers interested in more details about different types of EMI and how they can interfere on electronic devices, we would recommend the following literature: [20–22].

It is worth noting the correlation between the failure mechanisms induced by ionizing radiation and EM interference on ICs. While the former failure mechanisms are induced by *physical chances in the matter* forming the integrated circuit (charge deposition on insulating layers, which basically changes threshold voltage of transistors and increases overall circuit leakage current), the latter failure mechanisms *degrade signal integrity*, which promotes signal propagation delay increase and ultimately, signal desynchronization with respect to clock, particularly at critical (long) circuit paths. Despite the fact these failure mechanisms are uncorrelated, it is easy to suppose and accept that, if combined they potentially increase the probability that the circuit will fail in a shorter period of time. For instance, consider that a circuit has cumulated a high radiation dose due to a long period of time exposed to total ionizing radiation. Thus transistor threshold voltage shifts and circuit leakage current increase are expected at a given amount. This degradation of circuit electrical parameters induces signal delay

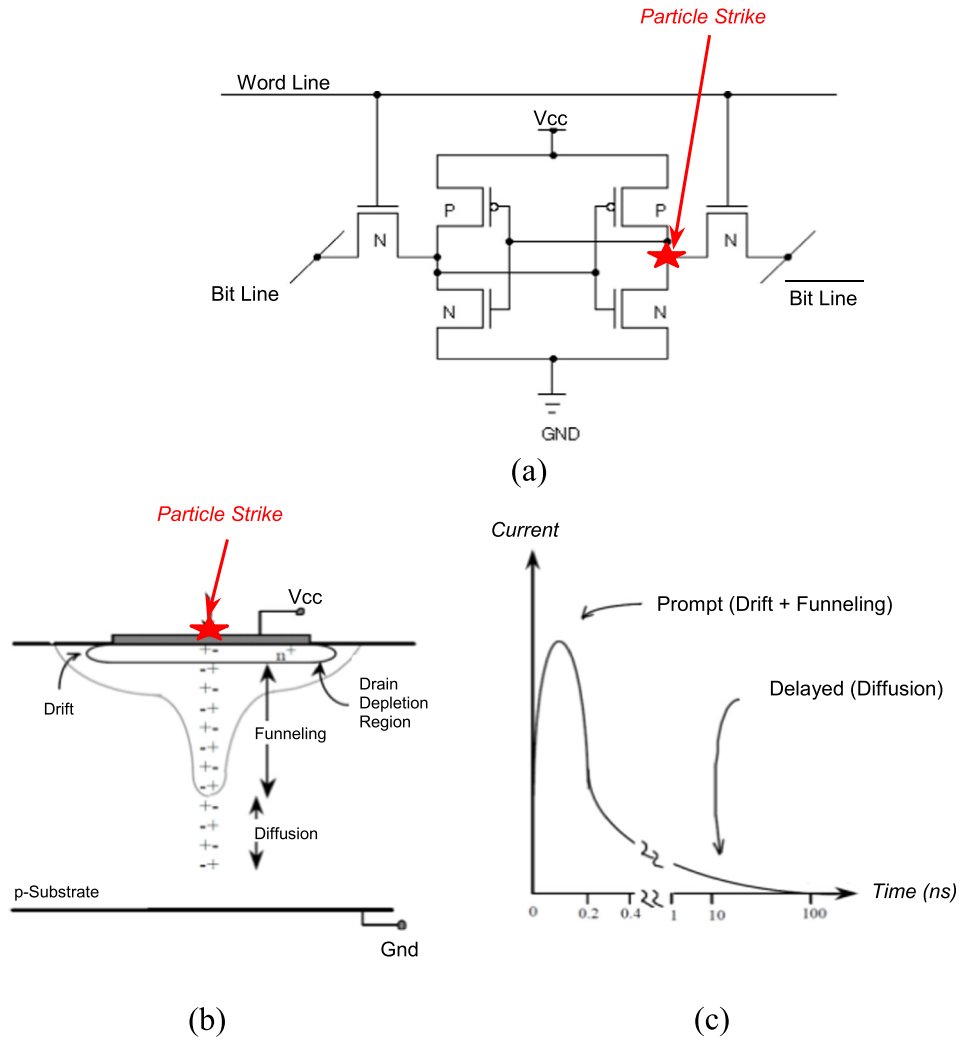


Fig. 2. Illustration of the mechanism by which a high-energy particle strike produces a bit-flip in a SRAM cell.

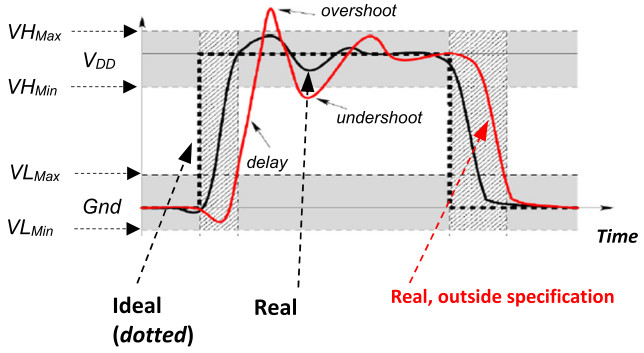


Fig. 3. Signal integrity degradation: signal outside noise margins can be erroneously interpreted and stored by memory elements placed at the end of critical paths.

propagation increase and ultimately, signal desynchronization with respect to clock at critical paths. In this scenario, it is easy to understand that if EM interference arrives at the d.c. input power port of such IC, the probability of signal desynchronization occurrence will increase. In this scenario, the IC is more prone to transient (and/or permanent) faults.

3. Proposed combined test for TID, SEU, EMI and laboratory setup

In order to measure the combined effects of both ionizing radiation and electromagnetic interference on ICs, we are proposing a combined test methodology that allows performing TID (and/or SEU) test of an IC simultaneously with the Conducted and Radiated EMI tests. Fig. 4 shows that the methodology allows performing TID (and/or SEU) test while the IC is being exposed to radiated and/or conducted noise on power supply lines. With this purpose, the combined test procedure and laboratory set up partially follows up international standards depicted in [6–12].

As observed in Fig. 4, the combined test starts by performing a functional test of the samples at nominal operating conditions, as ruled by the sample fabricant. The goal of this step is twofold: (a) check if the samples are fully operational and (b) perform a characterization test in order to take note of the electrical parameters' characteristics of the device (such as maximum operating frequency, minimum operating voltage, maximum power dissipation, temperature, etc.). Once this preliminary step is done, the combined test can be started. First, the SEU Test is performed by combining it with Conducted and/or Radiated Tests. Note that if Radiated Test (GTEM test method) is selected, then the SEU Test cannot be realized in a heavy-ion accelerator such as a Pelletron because the device under test, in the SEU Test, must be placed in a vacuum chamber (see Fig. 6). However, the vacuum chamber cannot be coupled with a GTEM cell where the Radiated Test is carried out. In order to overcome this problem, instead of a heavy-ion

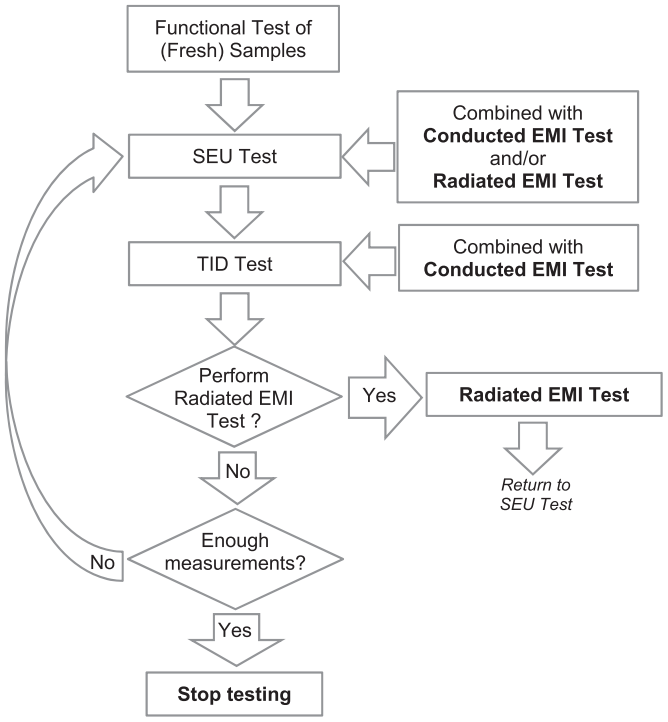


Fig. 4. Proposed combined test methodology.

accelerator, test engineers should use a ^{241}Am (Americium) source. Contrarily to heavy-ions, ^{241}Am source test can be performed at air atmosphere. Nevertheless, the GTEM cell must be adapted to properly receive the ^{241}Am source inside it. Another option is to apply neutrons' testing instead of heavy-ion or ^{241}Am source. Neutrons are one of the main sources of concern of soft errors in electronic systems devoted to avionics applications. Note that in this type of test, the GTEM cell must also be adapted to receive the neutrons source inside it.

Note that TID Test cannot be (simultaneously) combined with Radiated EMI Test. This is because of safety reasons, since ^{60}C source or any other similar type of (high-level) radiation source cannot be placed inside the GTEM cell. However, this is not important since TID Test is cumulative on the electronics and thus, if desired, Radiated EMI Test can be performed up to a few hours after the TID Test has finished, as a stand-alone step, since the expected dose rate is already deposited on the circuit. Thus, in practice, TID Test can be combined with Radiated EMI Test.

Finally, note that the SEU Test must be realized before the TID Test. This is mandatory because the former type of test is not destructive (it produces only transient faults in memory elements such as flip-flops and RAM cells such as described in previous section), but TID Test yields a given level of radiation dose to be permanently cumulated on the device under test, which is indeed destructive, not reversible. So, if one intends to analyze, for instance, how the combined effects of TID and Conducted EMI degrade the SEU sensitivity of the device under test, first of all he/she should perform an initial SEU Test + Conducted EMI Test without TID. This procedure is necessary to isolate the effects of TID from the effects of Conducted EMI on the device's SEU sensitivity.

During the realization of any of these test combinations, functionality and electrical parameters of the sample under test are monitored online, while test data logs are generated and stored for further analysis. When the size of the collected data is large enough to guarantee a minimum confidence level for the measurements, the combined test can stop.

Fig. 5 illustrates the TID test procedure on an X-Ray Diffractometer combined with conducted EMI test on power supply lines of an IC

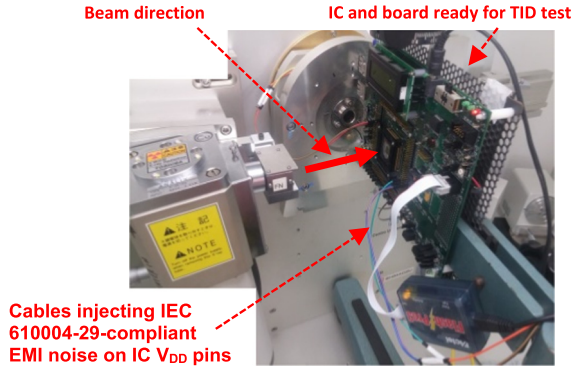
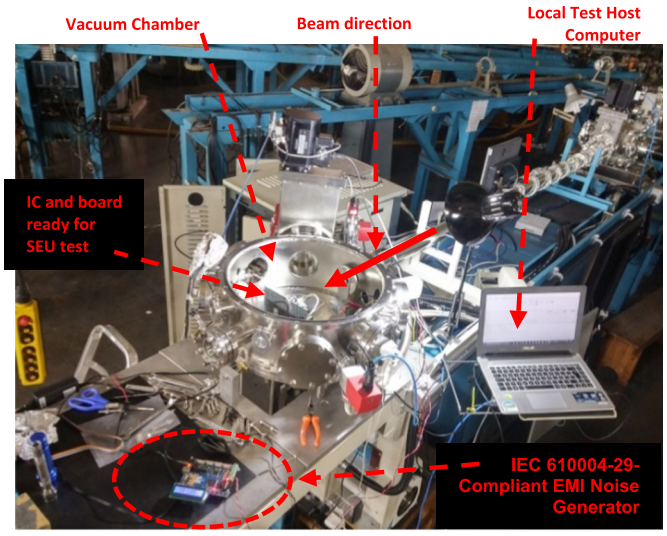
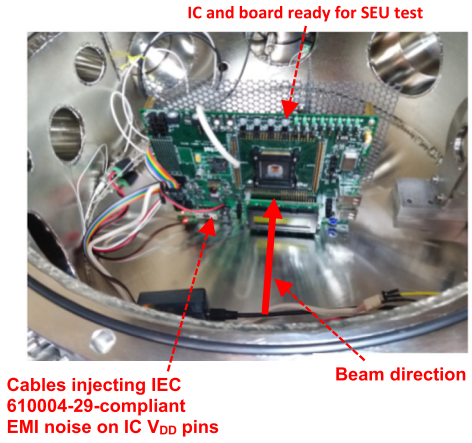


Fig. 5. Combined TID and conducted EMI test based on X-ray diffractometer equipment and noise injected directly on the V_{DD} input power pin of the IC.



(a)



(b)

Fig. 6. Combined SEU and conducted EMI test based on the pelletron heavy-ion accelerator equipment and noise injected directly on the V_{DD} input power pin of the IC according to the IEC 61000-4-29 std.: (a) general view of the test setup; (b) detail of the IC under test inside the vacuum chamber.

(Microsemi ProAsic3E A3PE1500 FPGA).

In the sequence, Fig. 6 depicts the combined SEU test of the same Microsemi FPGA on a Pelletron Heavy-Ion Accelerator with Conducted EMI Test on power supply lines. Note in Fig. 6b that the device under

test should have its package opened in order to expose the bare die directly to the ion beam. Opening the package is a mandatory procedure previously to perform SEU Test in order to allow the particles' detector, placed right beside the device under test inside the vacuum chamber, to properly count the number of particles incident on the bare die surface (and so, compute the flux and fluency parameters of the SEU Test).

4. Combined test experimental results – a case study on a |microsemi ProAsic3E A3PE1500 FPGA

This section describes the experiment and the obtained results of combining tests for SEU and Conducted EMI.

It is worth commenting that despite Fig. 4 shows a step with combined TID and EM interference at once radiated and conducted, in this section we only present SEU results combined with conducted noise injection because the goal hereafter is just to give the reader an example of how the combined test methodology could be applied and the importance of the results that can be obtained from using it. For all other possible combinations of test (TID and/or SEU and/or Conducted EMI and/or Radiated EMI), interested readers can address [14,15].

Fig. 7 depicts combined test results for heavy ions on the Pelletron Accelerator and conducted noise on 1.5-volt power supply pin of the FPGA that feeds energy to the core of the chip. The remaining power pins (2.5 and 3.5 V) feeding energy to the periphery logic of the chip remained noise-free. The applied noise was in the form of 10.38% voltage dips according to the IEC 610004-29 std (see Fig. 8). The choice for this noise level was based on the fact that this was the minimum voltage value that could be applied to the chip before we observed functionality loss, i.e., the system crash. The experiment setup for this combined test is as previously depicted in Fig. 6.

As seen in Fig. 7, the 10.38% injected noise on the V_{DD} pins of the chip degrades SEU immunity much more than merely applying a continuous 10.38% reduced V_{DD} (i.e., 1.34 V) when compared to the SEU immunity measured for the chip while operating in nominal conditions (V_{DD} = 1.5 V). For instance, when LET = 15 MeV, the number of observed errors per cm^2 is 2.2×10^{-3} for the nominal V_{DD}, while it is 2.57×10^{-3} when noise is applied to the chip and 2.4×10^{-3} when only a continuous reduced V_{DD} is injected on the power line. In this case, the injected 10.38% noise produced degradation on the SEU immunity of the FPGA on the order of **16.82%** while this number is **9.09%** for the case of V_{DD} reduction. For those readers not familiar with the "LET" measurement unit, this stands for "Linear Energy Transfer"; it is measured in terms of "Mega-Electron Volt" and it describes the energy deposited by an incident particle when crossing the substrate of the integrated circuit. So, as greater is the LET, larger is the deposited energy and so, greater is the probability of producing an SEU in a memory element inside the chip. Moreover, the parameter "Errors/Fluency (cm^2)" stands for the number of bit-flips observed in memory elements of the FPGA per second per square centimeter during a given experiment.

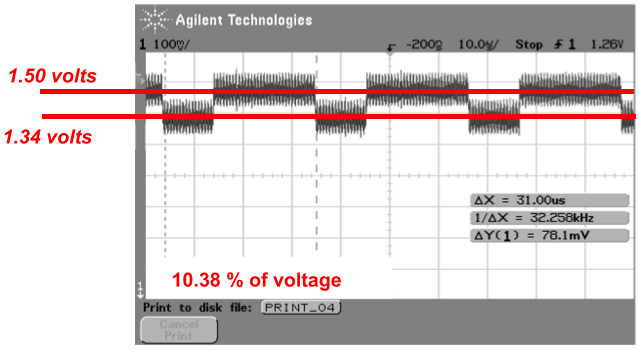


Fig. 8. 10.38% injected noise at the FPGA 1.5 V power bus (conducted EMI according to IEC 610004-29 std).

Fig. 9 summarizes SEU immunity degradation for the injected noise and reduced V_{DD} operating conditions with respect to the FPGA SEU immunity measured when nominal V_{DD} is considered. In this case, SEU immunity degrades in average by **13.89%** for the reduced V_{DD} with respect to the nominal V_{DD} (average number of observed errors per cm^2 increased by a factor of 2.25×10^{-4}, with respect to an averaged number of observed errors per cm^2 equal to 1.62×10^{-3} for nominal V_{DD}). On the other hand, SEU immunity degrades in average by a factor of **23.15%** when 10.38% noise is injected (average number of observed errors per cm^2 increased by a factor of 3.75×10^{-4} with respect to an averaged number of observed errors per cm^2 equal to 1.62×10^{-3} for nominal V_{DD}). In summary, one can conclude from this figure that conducted EM interference (as represented by the injected 10.38% noise on the d.c. input power port) is much more harmful to the IC SEU immunity than a simple reduction of V_{DD} operating conditions.

Finally, Fig. 10 analyses the influence of the type of noise injected in the FPGA input power pins on the SEU immunity. With this purpose, four noise signals with different frequencies (with the shape seen in Fig. 8 and with duty cycle of 50%) were injected in the FPGA, one at a time, in a separate experiment: 5 kHz, 50 kHz, 500 kHz and 1.5 MHz. As observed in this figure, the FPGA SEU sensitivity varies from 1.51×10^{-3} to 1.58×10^{-3}, implying a mean variation in the order of 4.53%.

From this experiment, we conclude that the frequency by which noise is injected in the FPGA input power pins (at least for the frequency range experimented) is not a parameter that should be taken in a great concern. Instead of that, the parameter that really matters for

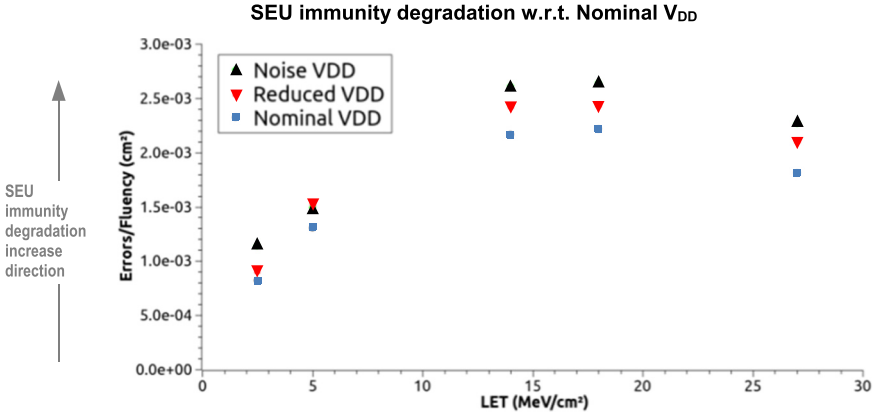


Fig. 7. SEU immunity measurements in the pelletron heavy-ion accelerator for the microsemi FPGA when combined with noise, without noise (nominal) and with reduced V_{DD}.

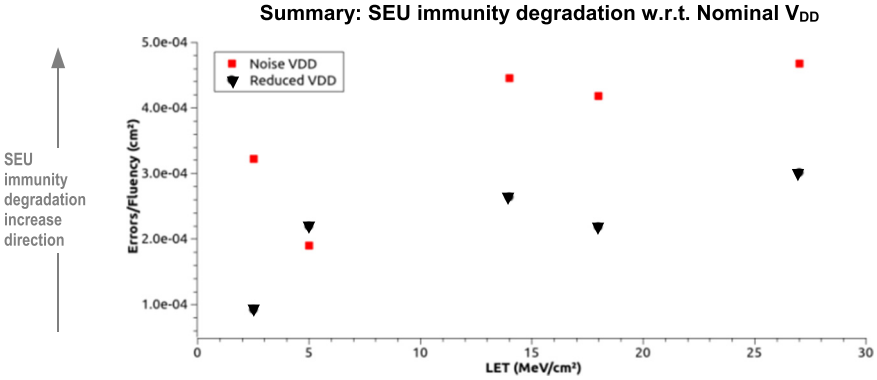


Fig. 9. Difference of the SEU immunity measurements for the "10.38% injected noise" and "continuous 1.34 V reduced V_{DD}" operating conditions, with respect to the FPGA SEU immunity measured at nominal V_{DD}.

SEU immunity is the fact that the input power pins of the chip are exposed or not to noise (which is more harmful to the chip reliability than when the device is operating with continuous reduced V_{DD} on the input power pins).

5. Discussion

As observed in Fig. 8, the ProAsic3E A3PE1500 FPGA experiment was based on the IEC 610004-29 std. According this standard, voltage dips can be injected in the d.c. input power port of the device under test at a frequency hanging from 1 Hz to 100 Hz (pulse duration from 0.01s to 1s) or at a frequency "x", which is an open value that can be defined by the user according application specificities. In this scenario, and as previously mentioned, we arbitrarily defined and injected in the FPGA four noise signals with different frequencies, one at a time, in a separate experiment: 5 kHz, 50 kHz, 500 kHz and 1.5 MHz. On the other hand, it is worth mentioning that at high frequencies, resonance mechanisms may appear and that would render the interference frequency a very important parameter. Considering this condition, future experiments will be based on other stds, such as the IEC 62132-3 Part 3: Bulk current injection (BCI) method, which rules measurement of electromagnetic immunity for a much larger bandwidth: [150 kHz–1 GHz]. In order to accomplish this goal, a more complex laboratory infrastructure (containing specific RF generator and amplifier modules and injection and monitoring probes among other components) will be needed when compared to the IEC 610004-29 std-based experiment we currently performed, which commonly sits around a quite simple test generator based on a programmable power supply, for instance. This more complex laboratory infrastructure has to be combined with SEU test running in a heavy-ion accelerator (Pelletron) by one side and TID test running in X-ray diffractometer equipment by other side. This will be an even more challenging experiment and this is the main reason we started the combined test experimentation by the IEC 610004-29 std one.

6. Conclusions

In the last decades, international standards have been proposed and used to test ICs for ionizing radiation (TID and SEU) as well as for electromagnetic interference (EMI). Nevertheless, these standards are applied to the IC or electronic system in a separate way, not taking into account the combined effects of these types of radiation may take over the ICs. From the best of our knowledge, there is no standard that rules combined tests for TID, SEU and EMI. In this scenario, this paper aimed to fulfill this lack of product quality information and suggested a new methodology to improve the reliability of ICs by performing combined tests for TID, SEU and EMI.

We also presented recent experimental results from combined measurements that we performed on a commercial FPGA IC (Microsemy ProAsic3E A3PE1500), which is widely used in critical embedded applications such as aerospace and automotive. These results have shown that the SEU immunity degraded by 23.15% when the IC is exposed to the combined effects of "SEU + Conducted EMI noise" on V_{DD} power supply lines as compared to when the IC is only exposed to SEU (operating at nominal V_{DD}). Therefore, the effects one type of radiation may take over the other are not negligible and should definitely be taken into account if one intends to design reliable embedded systems.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgements

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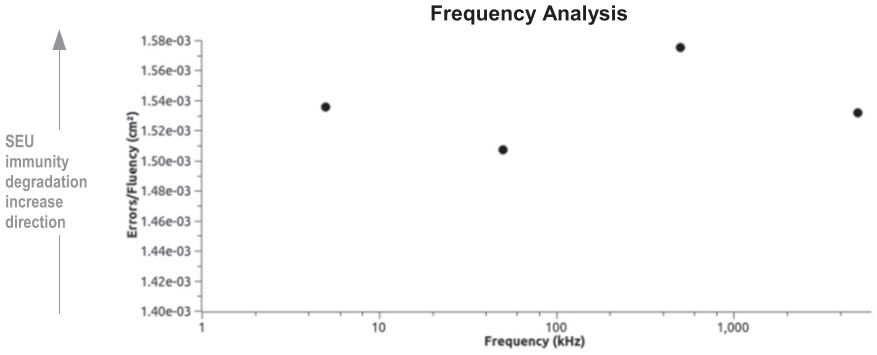

Fig. 10. Influence of the type of the noise injected in the input power pins of the FPGA on the SEU immunity.

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