Analysis of Conducted-EMI Noise Influence on the Effectiveness of an EDAC Technique to Mitigate Soft Errors in Ionizing Radiation Environment

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***Abstract*— This work describes preliminary experiments that analyze the influence of conducted electromagnetic interference (EMI) noise on the effectiveness of an error detection and correction (EDAC) technique. This technique was originally conceived to mitigate multiple-bit upsets (MBUs) or soft errors in memory elements (flip-flops and SRAM cells) of integrated circuits (ICs) operating in heavy ions environment. The analysis was performed on a Microsemi ProASIC3E A3PE1500 FPGA, which was operating in an 8MV Pelletron heavy-ion accelerator while exposed to conducted EMI noise on IC input power port. Injected noise comprised of voltage dips of 19.6% of V_{DD} at the frequency of 5kHz and was performed according to the IEC 61000-4-29 standard. The obtained results suggest that the proposed technique is very effective to detect and correct multiple bit flips induced by the combined effects of ionizing radiation and conducted EMI on the tested IC input power port.**

***Index Terms* — EDAC technique, Single-event upset, Combined effects, Ionizing radiation, Conducted EMI, ProASIC3E A3PE1500 FPGA, Power-supply noise.**

I. Introduction

The semiconductor industry advances to increase the computation throughput, reduce the size and improve power efficiency of Integrated Circuits (ICs). Still, the miniaturization of ICs renders them more susceptible to changes from external environment, such as electromagnetic interference (EMI) and ionizing radiation [1]. When considering the dimensions of today's semiconductor manufacturing technologies, the circuit can be affected by radiation even at the sea level [2]. These effects can cause temporary failures leading the system to an unwanted state.

Remarkably, Moore's Law still applies to current IC industry, meaning that it is possible to have large amounts of memory inside an IC, such as Static RAMs (SRAMs) cells and Flip-Flops (FFs). Nonetheless, besides improving the processing performance, reducing power consumption and increasing logic density, there must be a concern for raising dependability of integrated circuits.

Radiation, such as alpha particles and heavy ions, can cause Single-Event Upsets (SEUs) in memory elements of an IC. These effects are one of the major concerns when considering space applications [3] because they can compromise the entire system. Indeed, it is expected that the system relays on memory to function, e.g. storing program data that it is supposed to be further executed by a processor.

Fault tolerance in semiconductor devices has been a significant issue since the first flaws were observed in space applications several years ago [4,5,6]. Since then, interest in studying fault-tolerant techniques in order to maintain integrated circuits operating in hostile environments has increased, driven by all possible applications of using radiation-tolerant circuits such as space missions, satellites, high-energy physical experiments, and other.

To guarantee such robustness, several techniques are currently used to protect memory components against SEU. These techniques typically sit around Error Detection and Correction (EDAC) codes. Nevertheless, such techniques present several degrees of success, where the designer has to trade-off between area, power, delay and error correction/detection efficiency. In other words, one can design a memory system with very high degree of error detection and/or correction capability, but at a prejudice of area, power and/or delay increase. Single Error Correction, Double Error Detection (SEC-DED) codes can be used to avoid data corruption caused by soft errors [7,8], protecting the memory against single errors. However, the presence of Multiple Bit Upsets (MBUs) are becoming more frequent with the evolution of the manufacture process [9,10,11], which renders traditional techniques useless to correct (or even detect) errors in memory arrays.

This work describes preliminary experiments that analyze the influence of conducted EMI noise on the effectiveness of an error detection and correction (EDAC) technique. This technique was originally conceived to mitigate MBUs in memory elements (flip-flops and SRAM cells) of ICs operating in heavy ions environment. The analysis was performed on a Microsemi ProASIC3E A3PE1500 FPGA (IC commonly used for automotive and aerospace applications), which was operating in an 8MV Pelletron heavy-ion accelerator while exposed to conducted EMI noise on IC input power port. The injected noise comprised of voltage dips of 19.6% of V_{DD} at the frequency of 5kHz and was performed

978-1-5090-5997-3/18/$31.00 ©2018 IEEE

according to the IEC 61000-4-29 standard [12]. The obtained results indicate that the proposed technique is very effective to detect and correct multiple bit flips induced by the combined effects of ionizing radiation and conducted EMI on the tested IC input power port.

II. EDAC Technique Description

The proposed approach is based on a combination of information and hardware redundancies. Fig. 1 depicts the general block diagram. In more detail, each memory word is divided into byte segments and a parity bit is associated to each of the segments (parity-per-byte approach). Then, the whole memory is duplicated (Primary Memory and the Redundant Memory).

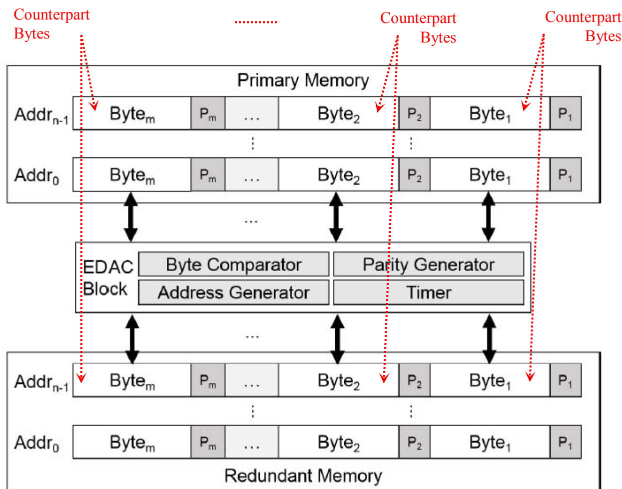


Fig. 1. General block diagram of the proposed EDAC approach.

In this scenario, when the processor performs a write operation, the EDAC Block computes the parity-per-byte of the written word and simultaneously writes the whole word, duplicated, into two separate memory areas. When the Wash process is initiated, the EDAC Block simultaneously reads both words from the two memory areas and performs the error analysis process as follows (see Fig. 2):

Step A) It compares both words on the byte-by-byte basis.

Step B) If any of the compared byte tuples does not match, the PBD approach annotates the byte position into the word.

Step C) Then, the parity-per-byte is computed for all bytes of both words.

Step D) If any of the parity-per-byte does not match, the approach annotates the byte position into the word.

Step E) Finally, the PBD approach combines the annotations generated in Steps B and D and corrects the erroneous word (if there is any) by copying the byte (or bytes) whose parity is correct into the byte (or bytes) whose parity is erroneous.

Step F) After performing steps (a) through (e), the PBD approach assumes that both words (stored into the Primary and Secondary Memories) are, at that current time instant, equal and correct, and writes them back to their respective duplicated memory areas.

Consideration C_1: Note that when the occurrence of a MBU that does not affect the parity of a byte (e.g., in the Primary Memory), at the same time that another bit upset affects the parity of the counterpart byte (in the Secondary Memory), then the PBD approach will erroneously copy the byte whose parity matched from the Primary Memory (even the byte contains MBU) into the byte whose parity did not match in the Secondary Memory in order to try to wash the memory. However, observe that both counterpart bytes in the Primary and in the Secondary Memories will contain errors at the end of this process. In such scenario, unfortunately, the considered MBU pattern escapes detection.

Consideration C_2: Note that when parities of both counterpart bytes do not match, the PBD technique detects the occurrence of error(s) in both bytes, but is not able to correct. In this scenario, only error detection is performed.

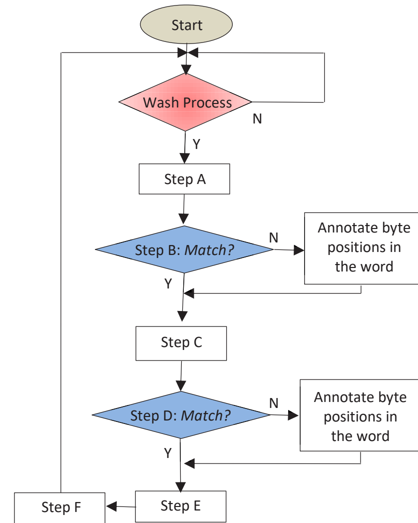


Fig. 2. Flowchart of the proposed EDAC technique.

The proposed approach yields one of the following four outputs:

- *No Error (NE)*: It is the default state; there is no error to be detected.

- *Error Detected & Corrected (EDAC)*: When a mismatch is identified upon comparing a byte and its counterpart. Then, the EDAC Block recalculates the parities simultaneously in these two memory bytes and assumes that the correct byte is the one whose parity checking is correct (true). Then, the EDAC Block performs error correction by simply copying such error-free byte over the one whose parity recalculation yielded an incorrect result.

- *Error Detected & Not-Corrected (EDNC)*: Similarly to the previous case, but no parity match is found as result of the simultaneous parity recalculation in both bytes. Therefore, the EDAC Block assumes that there is at least one error in each of the considered bytes, but the EDAC Block cannot correct it because both parity bits are wrong (false).

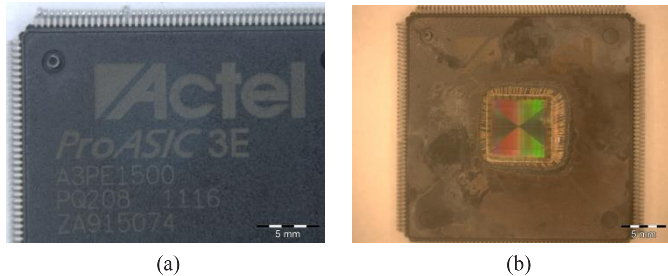
- *Error Not-Detected & Not-Corrected (ENDNC)*: This is the worst-case scenario. As described in Consideration C_1, when the occurrence of a MBU that does not affect the parity of a byte (e.g., in the Primary Memory), at the same time that

another bit upset affects the parity of the counterpart byte (in the Secondary Memory), then the PBD approach will erroneously copy the byte whose parity matched from the Primary Memory (even the byte contains MBU) into the byte whose parity did not match in the Secondary Memory in order to try to wash the memory. However, observe that both counterpart bytes in the Primary and in the Secondary Memories will contain errors at the end of this process. In this scenario, unfortunately, the considered MBU pattern escapes detection.

III. Combined Test for SEU/Conducted EMI

Hereafter, the experiment performed to analyze the error detection and correction capability of the proposed approach under combined effects of ionizing radiation and EMI is described.

The device under test (DUT) was a ProASIC3E FPGA model A3PE1500, which is cost-optimized: reprogrammable and nonvolatile. It is based on flash technology to store configuration bits, whereas volatile memory (in the form of flip-flops and SRAM cells) is used to store user data [13]. Some other A3PE1500 device important characteristics for safe, critical applications are: (a) it supports 128-bit AES decryption for device configuration, (b) it is single chip and live at power-up and (c) 1,024 bits of user flash memory. In order to properly perform SEU radiation test according to the MIL-STD 883H Method 1019.8 [14], the FPGA package was opened by means of a chemical/mechanical process. Fig. 3 shows the final state of the open-cavity die.



(a) (b)

Fig. 3. Microsemi ProAsic3E A3PE1500 FPGA: (a) Packaged device; (b) Unpacked, ready for radiation (SEU and TID) tests.

The FPGA was configured with a dedicated logic written in *VHSIC Hardware Description Language* (VHDL). This logic was split into parts: the first part mapped the PBD technique described previously, whereas the second part mapped flip-flops (FFs) and SRAM cells as a single array of memory elements that were serially accessed (First-In-First-Out, FIFO). The FFs and SRAM cells were mapped with two specific patterns: *all 0's* and *all 1's*. At the beginning of the experiment, all memory elements were initialized with the logical pattern "0". Then, after all measurements were done for this pattern, i.e., all FFs and SRAM cells addresses have been read out, all FFs and SRAM cells were reset and fulfilled with the logical pattern "1". These patterns were selected for two reasons:

a) to have full control of all data stored into the FPGA memory elements (FFs and SRAM cells) and

b) to observe if the FPGA sensitivity is similar for bit-flips from "0" to "1" and from "1" to "0".

The used design framework was the Microsemi *Libero* tool. Also from Microsemi, the *FlashPro* tool was used to download the configuration bit-stream, as well as to read/write process of the FF and SRAM array via JTAG interface during the whole experiment.

Table I summarizes the ProASIC3E resource usage for the experiment and the maximum resources available for the device. The hardware configuration mapped the total allowable SRAM cell storage capacity of the FPGA. In this case we addressed 276,480 SRAM bits, which comprised of 15,360 addresses. Each SRAM address represents an 18-bit wide structure.

Table I. ProAsic3E occupied resources

FPGA Hardware Summary	Core Logic (VersaTiles)	FFs	SRAM Cells
Used hardware configuration	37,903	18,432	276,480
Max. hardware available	38,400	38,400	276,480

Contrarily to SRAM cells that are placed in a separate area of the FPGA die, FFs are sitting and homogeneously distributed in the Core Logic (named VersaTiles by Microsemi). In such logic, we occupied 18,432 FFs, which represented 48.63% of the total number of available FFs (38,400) in the FPGA. These 18,432 FFs were spread around 98.71% (37,903) of the VersaTiles area and were directly accessed from the host test computer via JTAG. The totality of 1,024 FF addresses was accessed, where each address represents an 18-bit wide structure.

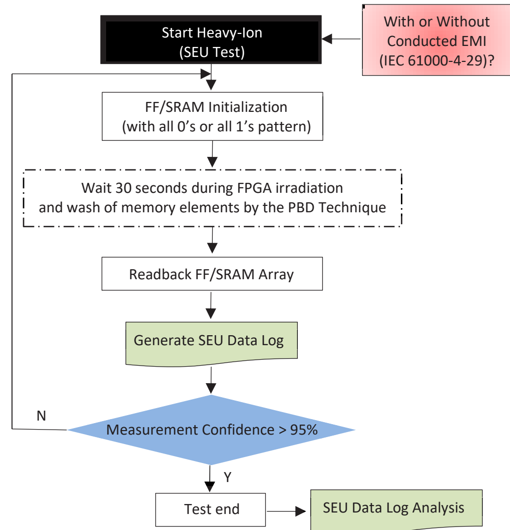


Fig. 4. Test Flow.

Initially, a functional test was performed to check the FPGA nominal operating conditions: minimum operating voltage (V_{DDmin}) and average dynamic current (I_{DDave}).

The whole test procedure depicted in Fig. 4 is described below:

- *Step 1*: Perform SEU test of the FPGA for the FF and SRAM array initialized with all 0's, with nominal V_{DD} (no EMI noise applied on the V_{DD} power bus);
- *Step 2*: Perform SEU test of the FPGA for the FF and SRAM array initialized with all 1's, with nominal V_{DD} (no EMI noise applied on the V_{DD} power bus);
- *Step 3*: Perform SEU test of the FPGA for the FF and SRAM array initialized with all 0's, with EMI noise applied on the V_{DD} power bus;
- *Step 4*: Perform SEU test of the FPGA for the FF and SRAM array initialized with all 1's, with EMI noise applied on the V_{DD} power bus;

For each of the FPGA configurations above, the FPGA remained exposed to heavy ions irradiation and/or EMI noise injection during a period of 30 seconds. During this time window, it was performed 3 readback processes (one at every 10 seconds) from the FPGA to the test host computer in order to analyze in the log files, bit-by-bit, the capability of the proposed EDAC technique to detect and correct errors in a hostile environment. Moreover, the time interval between two wash procedures of the memory was set to 1/second. In more detail, after a 30-second time window, the memory was fully washed 30 times by the PBD technique. Similarly, a readback process was performed at every 10 wash procedures of the memory.

The steps depicted in Fig.4 were repeated till we had a confidence on the measurements equal to or greater than 95%. When this amount was reached, the generated SEU data log was analyzed.

SEU Test:

The Single-Event Upset (SEU) test was performed by exposing the ProASIC3E FPGA to 5.4 MeV alpha particles emitted by a ^{241}Am source. The alpha-particle flux was about 13.7 particles per second per millisteradian (part/s/msr) [15]. Fig. 5 depicts the basics of the test setup.

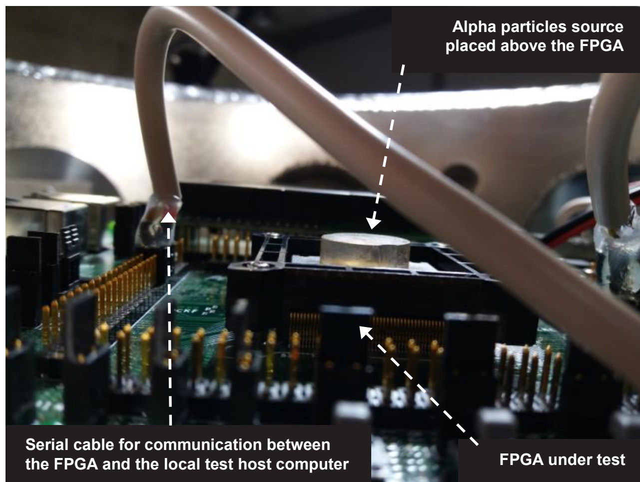


Fig. 5. Test setup for the ^{241}Am source.

EMI Test:

Fig. 6 depicts the noise injected in the V_{DD} power supply lines of the FPGA. Fault injection campaigns were generated according to the IEC 61000-4-29 standard [12] by applying voltage dips to the core V_{DD} pins of the FPGA. The nominal core V_{DD} is 1.5 volts. During the experiment, the IC peripheries remained fixed at their nominal voltage levels, i.e., 3.3, 2.5 and 1.8 volts. Voltage dips were randomly injected at the V_{DD} input pins at a frequency of 5 kHz (50% duty cycle) and consisted of dips of about 19.60% of the nominal V_{DD}. In this case, the voltage at the core V_{DD} oscillated between 1.53 and 1.23 volts. For voltage dips larger than this value, we observed the FPGA collapsed, i.e., it was not functional any more.

It is worth mentioning that the IEC 61000-4-29 method was selected as a meaning for injecting noise on the FPGA mainly because of its simplicity (i.e., ease of implementation) associated to the need of low-cost equipment for noise generation. Moreover, its low complexity yields this method to be easily reproduced at different laboratories with a high degree of confidence.

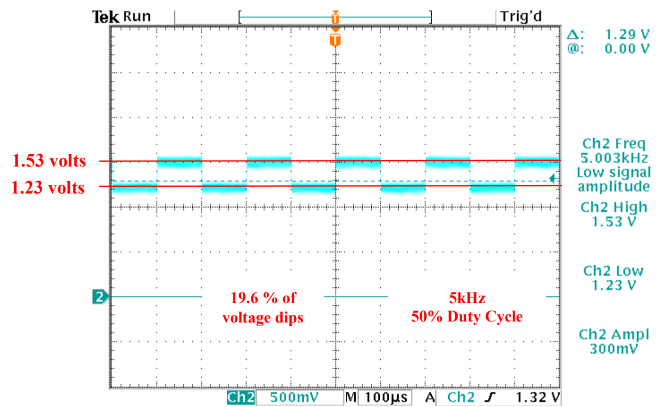


Fig. 6. Noise injected on FPGA V_{DD} pins.

IV. OBTAINED RESULTS

Tables II and III present results for the heavy-ion test with and without conducted EMI on the core power supply bus of the FPGA. Table II summarizes results for the SRAM cells array, while Table III displays results for the FFs of the FPGA.

As observed in both tables, the following conclusions can be taken:

i) The proposed technique is able to detect and correct the vast majority of bit flips in memory elements (SRAM cells or FFs), no matter the soft errors are the consequence of heavy ions themselves, or such errors are produced by the combination of heavy ions and conducted noise on the input power port of the FPGA.

ii) According to the measurements, the latter case (i.e., when exposing the system to the combined effects of heavy ions and conducted noise), the memory system becomes in average 2.7 times more sensitive to soft errors, which is not a negligible number and should be taken into account by

engineers when designing robust electronic systems for critical applications such as aerospace.

TABLE II. CAPABILITY OF THE PBD TECHNIQUE TO MITIGATE SOFT ERRORS INDUCED BY HEAVY IONS, WITH AND WITHOUT CONDUCTED EMI NOISE ON THE CORE INPUT POWER PORT OF THE FPGA. RESULTS FOR THE **SRAM CELL** ARRAY.

PBD TECHNIQUE EFFECTIVENESS TO HEAVY IONS, WITH AND WITHOUT CONDUCTED EMI NOISE ON INPUT POWER PORT			
Average number of…	Without Noise	With Noise	Soft Error Increase*
observed bit-flips	395.00	1,049.00	2.7
bit-flips per memory bits	0.0027	0.0071	2.6
bit-flips per second	0.4760	1.0708	2.3
bit-flips per memory bits per second	0.0028	0.0073	2.6
addresses corrected**	393.33	1,044.37	2.7
addresses not corrected	0.17	0.63	3.7
masked addresses***	0	0	0
EDAC Effectiveness (%)	99.96	99.94	

* *"Soft Error Increase" rate was computed as: With Noise/Without Noise.*

** *the number of addresses corrected is smaller than the number of observed bit-flips because there was at least one address with more than one bit flip.*

*** *masked addresses are addresses not detected and not corrected, thus escaping detection by the proposed technique.*

TABLE III. CAPABILITY OF THE PBD TECHNIQUE TO MITIGATE SOFT ERRORS INDUCED BY HEAVY IONS, WITH AND WITHOUT CONDUCTED EMI NOISE ON THE CORE INPUT POWER PORT OF THE FPGA. RESULTS FOR THE **FF** ARRAY.

PBD TECHNIQUE EFFECTIVENESS TO HEAVY IONS, WITH AND WITHOUT CONDUCTED EMI NOISE ON INPUT POWER PORT			
Average number of…	Without Noise	With Noise	Soft Error Increase*
observed bit-flips	32.83	85.00	2.6
bit-flips per memory bits	5.4722	53.1250	9.7
bit-flips per second	0.0338	0.0867	2.6
bit-flips per memory bits per second	5.6414	54.2091	9.6
addresses corrected**	31.83	85.00	2.7
addresses not corrected	0	0	0
masked addresses***	0	0	0
EDAC Effectiveness (%)	100.00	100.00	

* *"Soft Error Increase" rate was computed as: With Noise/Without Noise.*

** *the number of addresses corrected is smaller than the number of observed bit-flips because there was at least one address with more than one bit flip.*

*** *masked addresses are addresses not detected and not corrected, thus escaping detection by the proposed technique.*

V. DISCUSSIONS

As mentioned in Section III, the experiment was performed for the FPGA exposed to heavy ions irradiation and/or EMI noise injection during a period of 30 seconds. During this time window, it was performed 3 readback processes (one at every 10 seconds) from the FPGA to the test host computer in order to analyze in the log files, bit-by-bit, the capability of the proposed EDAC technique to detect and correct errors in a hostile environment. Moreover, the time interval between two wash procedures of the memory was set to 1/second. Therefore, during a 30-second time window, the memory was fully washed 30 times by the PBD technique; and a readback process was performed at every 10 wash procedures of the memory. In such configuration, the measured efficiency was 99.94% (when the FPGA was exposed to the combined effects of heavy ions and noise on the power bus). For future work, we are preparing an experiment that provides us information on which is the maximum time interval between two wash procedures that guarantees 99.94% reliability. We think that it is quite possible that such maximum time is much larger than 1/second, which is very positive. This is positive because as large is the time interval between two wash procedures, smaller is the PBD approach intervention in memory, so freeing this infrastructure to be accessed by the processor at any time, which minimizes the possibility of system performance degradation due to the use of the proposed technique.

Additionally, it would be interesting to analyze the proposed technique efficiency under the combined test of heavy ions and another types of injected noise on the IC input power port, such as those generated according to the standards IEC 61000-4-17 (ripple on V_{DD}) and IEC 62132-3 (bulk current injection – BCI method) and IEC 62132-4 (Direct Power Injection – DPI method), among others. In other words, we intend to analyze the dependency of the proposed technique to the type of injected noise on the input power port.

VI. CONCLUSIONS

This work analyzed the influence of conducted EMI noise on the capability of an error detection and correction (EDAC) technique to counteract with multiple bit upsets (MBUs) in memory elements (flip-flops and SRAM cells) of ICs operating in heavy ions environment. The study was performed on a Microsemi ProASIC3E A3PE1500 FPGA (IC commonly used for automotive and aerospace applications), which was operating in an 8MV Pelletron heavy-ion accelerator while exposed to conducted EMI noise on IC input power port. The injected noise comprised of voltage dips of 19.6% of V_{DD} at the frequency of 5kHz and was performed according to the IEC 61000-4-29 standard. This method was selected as a meaning for injecting noise on the FPGA mainly because of its simplicity (i.e., ease of implementation) associated to the need of low-cost equipment for noise generation. Moreover, its low complexity yields this method to be easily reproduced at different laboratories with a high degree of confidence.

The obtained results indicate that the proposed technique is very effective to detect and correct multiple bit upsets even when the memory is exposed the combined effects of ionizing radiation and conducted EMI on the tested IC input power port.

Moreover, according to the measurements, when exposing the FPGA to the combined effects of heavy ions and conducted noise, the memory system, composed of FFs and

SRAM cells, became in average 2.7 times more sensitive to soft errors, which is not a negligible number. We expect engineers should take into account this conclusion when designing robust electronic systems for critical applications such as aerospace.

ACKNOWLEDGEMENTS

This work has been supported in part by CNPq (National Science Foundation, Brazil) under contract n. 306619/2015-6 (PQ), Project CITAR-FINEP, FAPESP (contract n. 2012/03383-5) and Instituto Federal do Rio Grande do Sul (IFRS).

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