A Hardware-Based Approach for SEU Monitoring in SRAMs with Weak Resistive Defects

G. Redivo Pinto, G. Cardoso Medeiros, F. Vargas, L. Bolzani Poehls
School of Engineering
Pontifical Catholic University of Rio Grande do Sul - PUCRS
Porto Alegre, Brazil
leticia@poehls.com

***Abstract*— CMOS technology scaling has made the increase of transistor density in Systems-on-Chip (SoC) possible. In addition, the necessity of storing more and more information has resulted in the fact that Static Random Access Memories (SRAMs) have become great part of the SoC's silicon area. This miniaturization brings up several benefits, among them an increase of system performance. However, some undesirable behaviors, that did not exist or that were negligible, now became reality. Manufacturing process variation has introduced new types of defects, such as: (1) Resistive-Open defects and (2) Resistive-Bridge defects, which depending on their size can cause static or dynamic faults. Indeed, the circuit's sensibility to environmental noise is another challenge related to technology scaling. In more detail, the interference can damage the circuit behavior and cause Single Event Upsets (SEUs), affecting the circuit's reliability. Given these circumstances, this work proposes a hardware-based methodology able to detect resistive defects as well as to monitor defective cells in field aiming to detect SEUs. The fundamental idea is to use part of the hardware introduced to perform the manufacturing test to also detect bit-flips during the circuit's lifetime. Note that only SRAM cells with weak resistive defects are monitored, since the cells with strong defects that propagate static faults are isolated after manufacturing test. The proposed work has been validated and evaluated through SPICE simulations adopting an SRAM array modeled with a commercial 65nm CMOS technology library.**

Keywords—SRAMs; Resistive-Open Defects; Resistive-Bridge Defects; Environmental Noise; SEUs, Hardware-Based Approach

I. INTRODUCTION

Advances in nanometer technology have made the integration of hundred million transistors into a small area, not larger than a few square centimeters, possible; allowing the increase of the circuits' density. In parallel, the always increasing need to store more and more information has resulted in the fact that Static Random Access Memories (SRAMs) occupy great part of the Systems-on-Chip's (SoCs') silicon area. In other words, memory has become the main contributor to the overall SoC area. The SIA Roadmap forecasted memory density approaching 94% of the SoC's silicon area for 2015 [1].

On the one hand, the most critical downside of technology scaling beyond the 65nm node is related to the non-determinism of the devices' electrical parameters due to process variation [7][8]. This type of variation is mostly caused by random fluctuations of dopant atoms and can be observed as a fixed deviation from the device's nominal behavior [9]. Thus, technology scaling has led to the development of new types of manufacturing defects that may assume a dynamic behavior. A resistive-open defect is defined as a defect resistor between two circuit nodes that should be connected [8]. A resistive-bridge defect creates a connection between two nodes that should have no relation and is caused by inconsistencies and imperfections in the manufacturing process [11]. In more detail, the new connection has a fixed resistance value that depends on its shape and the materials involved. Note that if the resistance of the new connection is sufficiently small, the circuit will be affected by a delay large enough to cause failures, which can be detected by traditional test methods. Nevertheless, if the resistance is not significantly small, the defect will not necessarily be able to cause a faulty behavior impacting the SRAM's reliability. These so-called weak defects generally cause timing dependent faults, which means that at least a 2-pattern sequence is necessary to sensitize them [5]. According to [4], faults requiring a large number of at-speed operations on each memory cell for sensitization are denominated dynamic faults.

On the other hand, inherent environmental noise may affect IC's behavior causing Single Event Effects (SEEs). Technology scaling has exacerbated the susceptibility of ICs to environmental noise, since the physical size of cells has been reduced implying on a scale-down in the junction area and a reduction in capacitance, leakage as well as operating voltage. In every generation, operating voltage and node capacitance decrease at a rate of 30%, representing an exponential drop in the charge used to represent a logic value [12]. Therefore, a small interference may already change the state of the cell. Thus, when environment noise, Electromagnetic Interference (EMI) or radiation, affects a memory cell, it can cause a Single Event Upset (SEUs) in the affected cell as well in neighboring cells. These bit-flips are produced by single charged particles that strike the transistor's drain. Particles liberate energy when hitting the ICs and produce electron hole pairs, creating a dense ionized track in the local region. Consequently, the ionization causes a transient current pulse, which can produce a SEU, consequently flipping the value stored in the cell. Until a new value is written, the wrong data remains stored.

In this context, the impact of SEUs on SRAM cells that have been affected by some kind of nominal behavior deviation

978-1-5386-1472-3/18/$31.00 ©2018 IEEE

caused by process variation associated to the manufacturing process is analyzed.

This paper proposes a hardware-based methodology able to detect resistive-open and resistive-bridge defects in SRAMs and to monitor SRAM cells with weak defects aiming to detect SEUs caused by environmental noise in field. In more detail, the idea behind the proposed approach is to use part of the already introduced hardware in order to perform the defective cells detection also to detect possible bit-flips in field. Note that the usually adopted test procedures are mostly designed for detecting static faults and not able to detect dynamic faults. In fact, the detection of dynamic faults poses significant challenges related to the necessity of performing at-speed testing as well as, depending on the defect size present in the SRAM cell, the obligation to execute a large number of operations on each memory cell. Basically, the defect size defines if a fault is classified as static or dynamic. Thus, some particular defects that may have not been detected during manufacturing test, may cause dynamic faults during the SRAM's operation in the field due to environment noise. Experimental results obtained through SPICE simulations using a commercial 65nm CMOS technology library demonstrated that the proposed methodology is able to detect weak resistive defects for a large range of defect sizes as well as its ability to detect bit-flips in most of the studied cases, while introducing tolerable overheads.

The paper has been organized as follows: in Section II the background related to SRAM as well as the assumed resistive-open and resistive-bridge fault models for SPICE simulations are described. Section III portrays the proposed hardware-based approach, whereas Section IV summarizes and discusses the obtained results and lays out an analysis of the introduced overheads. Finally, Section V presents the final considerations of this work.

II. Background

As previously mentioned, process variation has led to the introduction of new manufacturing defects that may generate dynamic faulty behaviors during the operation of defective cells. Indeed, SEUs have emerged as one of the most important sources of transient faults on memory cells due to the technology miniaturization. Thus, in this Section, the main characteristics of the SRAM cell and the fault models adopted to represent resistive-open and resistive-bridge defects in SRAM cells will be described.

A. The SRAM Cell

A standard six-transistor SRAM cell, composed of four transistors that form two cross-coupled CMOS inverters and two nMOS transistors that provide read and write access to the cell, is adopted in this work. The transistor sizing has been determined to be a reasonable trade-off between cell density and robustness. This choice results in the following transistor sizing values: (a) The ratio between pull-down and access transistors (Rd), where Rd = Wpull-down/Waccess = 0.18nm/0.12nm = 1.5; and (b) the ratio between pull-up and access transistors (Rp), where Rp = Wpull-up/Waccess = 0.20nm/0.12nm = 1.67. Note that these values assure the SRAM cells' stability against a noise of 200mV during read operations. Finally, the basic SRAM cell has been mapped into a commercial 65nm CMOS technology library.

B. Fault Model Associated to Resistive Defects

During the manufacturing process, a standard six-transistor SRAM cell can be produced including resistive defects that may modify the correct behavior of the memory cell. Resistive-open defects can be functionally characterized according to fault model presented in [11] and resistive-bridge defects according to the fault model described in [13]. In more detail, these fault models represent the set of the following faulty behaviors:

- *Stuck-at Fault* (SAF): A cell is said to have an SAF when it is unable to store both logic values. *Stuck-at 1* represents a cell that cannot store logical value '0', while *Stuck-at 0* represents the opposite.
- *Read Destructive Fault* (RDF): A cell is said to have an RDF if a read operation performed on the cell changes the data in the cell and returns an incorrect value on the output. Note that this type of fault can also have a dynamic behavior, being classified as dRDF;
- *Deceptive Read Destructive Fault* (DRDF): A cell is said to have a DRDF if a read operation performed on the cell returns the correct logic value, and it changes the contents of the cell. This type of fault can also have a dynamic behavior classified as dDRDF;
- *Incorrect Read Fault* (IRF): A cell is said to have an IRF if a read operation performed on the cell returns an incorrect logic value, and the correct value is still stored in the cell;
- *Weak Read Fault* (WRF): A cell is said to have a WRF when the ΔV between inverters is not enough for the sense amplifier to produce the correct logic output;
- *Transition Fault* (TF): A cell is said to have a TF if it fails to undergo a transition from '0' to '1' or vice versa when it is written.

As previously mentioned, a fault classified as dynamic is caused by a resistive defect that demands a write operation followed by multiple sequential read operations in order to sensitize the faulty behavior [13]. The number of read operations depends on the defect size. It is important to highlight that the last two described faults occur only in the presence of resistive-bridge defects. Fig. 1 depicts the scheme adopted to model the previously described faults associated to resistive-open defects. This model is based on the injection of 5 defects in different positions of the SRAM cell. According to [14], TFs can be modelled using Df1, Df5 or Df6. RDF or dRDF can be observed injecting Df2, Df3, Df4, Df5 or Df6. Indeed, DRDF or dDRDF can be modelling using Df2, Df3 or Df4. Finally, IRF is caused exclusively by Df5. It is important to highlight that the faulty behaviors associated to each defect reported in [14] differ from the ones identified in this paper. Due to the reduced defect size range adopted during the simulations, the number of faults related to each defect may not reach the complete set of faults reported in [14].

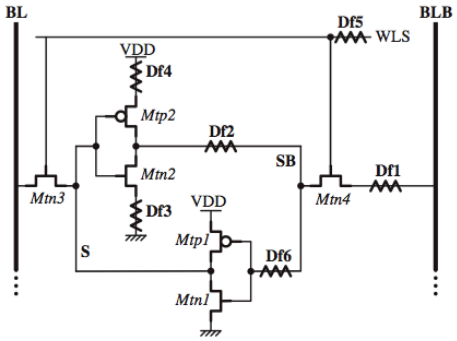

Fig. 1. Resisitive-open defects injected into an SRAM cell [11].

Regarding resistive-bridge defects, Fig. 2 depicts the scheme adopted in order to model these defects.

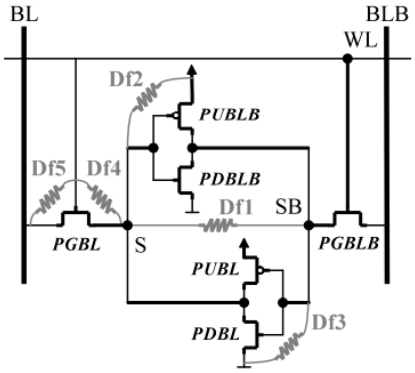

Fig. 2. Resisitive-bridge defects injected into an SRAM cell [13].

The five resistive-bridging defects can be classified into two distinct groups [13]:

- *Group_1:* This group includes defects that may affect the behavior of the core-cell when read and/or write operations are performed on it. Defects associated to Group_1 involve single-cell faulty behaviors and include Df1, Df2 and Df3. Thus, these defects may impact electric nodes within the core-cell only;
- *Group_2:* This group includes defects affecting the behavior of the defective core-cell and of other non-defective core-cells of the array. Defects associated to Group_2 may involve double-cell faulty behaviors. Group_2 includes Df4 and Df5, as these defects may impact BL and WL nodes.

According to [13], SAFs can be modeled using Df2, Df3 or Df4. RDF or dRDF can be observed injecting Df1, Df2, Df3, or Df5. There are no reports of DRDF or dDRDF with the injection of these defects. Finally, IRF can be caused by Df4 or Df5, while WRFs can be modeled using all defects described. It is important to highlight that the faulty behaviors associated to each defect reported in [13] differ from the ones identified in this paper. Due to the exhaustive simulations performed in this work, additional faults related to each defect complement the set of faults reported in [13].

III. The Proposed Hardware-Based Approach

The hardware-based approach proposed in this paper aims to detect resistive defects during manufacturing test as well as to monitor SRAM cells' behavior in field in order to detect the occurrence of SEUs. The main idea is to use the hardware presented in [14] in order to perform the manufacturing test also to monitor SRAM cells with weak defects, since they can exacerbate the cell's susceptibility to bit-flips. In more detail, the proposed approach is based on three main functional blocks: (1) Defect Sensors, (2) Bit-Flip Sensors and (3) Controller Block. Fig. 3 depicts the block diagram of a SRAM array with the hardware-based approach.

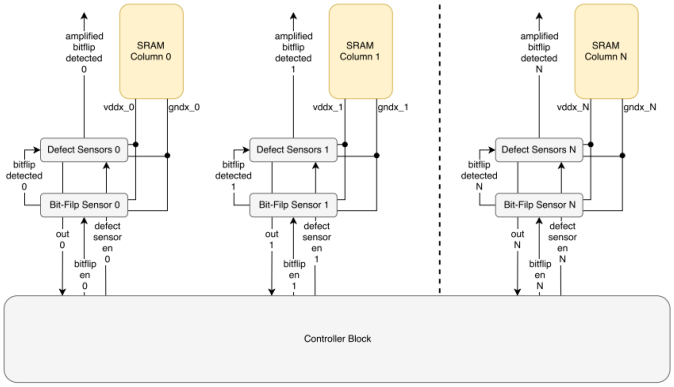

Fig. 3. Block diagram of the proposed approach.

The set of Defect Sensors monitors the current consumption of all cells present in the same SRAM array row to identify the eventual existence of defective cells using a neighborhood comparison logic. The Bit-Flip Sensors are able to sense the current consumption of a SRAM column in order to identify bit-flip occurrence. However, it is important to point out that the Bit-Flip Sensor's output needs to be amplified by the Defect Sensors' OPAMP. The identification of bit-flips is possible because a large peak of current at power lines can be observed when a bit-flip occurs in the cell. Note that the proposed approach is based on the insertion of a Bit-Flip Sensor for each monitored SRAM line. Finally, the Controller Block is responsible to manage, based on the Defect Sensor's output, when the column's Bit-Flip Sensor need to be enabled. Furthermore, the Defect Sensors must be disabled after performing the test procedure necessary to identify the cells that need to be monitored for the same purpose.

Fig. 4 shows the block diagram of the hardware-based approach, detailing the three functional blocks described above. There are five interconnected blocks, that together are responsible for detecting the resistive defects, for monitoring the cell's behavior in order to identify the occurrence of bit-flips, as well as for controlling the circuit's functionality during manufacturing test and SEUs monitoring. In more detail, the GND Defect Sensor and VDD Defect Sensor are responsible for sensing the power lines and to generate the PWM signal of all 8 bits of SRAM, summing 16 signals: 8 for GND and 8 for VDD. This PWM signals will be handled by the Full Detection Logic (FDL), which processes the PWD and pulses its output when some fault was detected. Those pulses are connected to the Latch Bank, which is responsible to store the information about which

columns contain defective cells, that is, which columns have to be monitored. The Bit-flip Sensor senses the power lines in order to identify bit-flips. The Bit-Flip Sensor's output is connected to the OPAMP of the GND Defect Sensor in order to amplify its value to a useful strength.

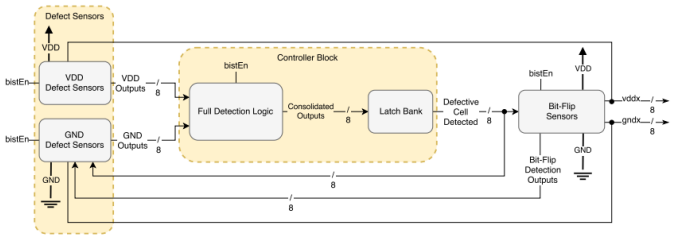

Fig. 4. Hardware-based approach block diagram.

Finally, it is important to highlight that the hardware-based approach has two distinct execution moments. Firstly, part of the introduced hardware, more precisely the Defect Sensors and the Controller Block, is used in order to perform a manufacturing test able to detect resistive defects independently from their magnitude. Secondly, the other part of the introduced hardware is used to identify SEUs that can affect SRAM cells. In more detail, the Bit-Flip Sensors are enabled for monitoring the SRAM cells with weak defects since they can exacerbate the cells susceptibility to bit-flips. Note that in field, the Defect Sensors remain disabled.

IV. Experimental Results

This Section summarizes the main results obtained during the simulations performed in order to evaluate the hardware-based approach proposed in this paper. Electrical simulations have been performed adopting an SRAM, composed of 8 lines of 8 columns each connected to the functional blocks, using a 65nm technological library by STMicroelectronics considering the corner defined as typical, with the temperature set to 27ºC and the voltage to 1.0V.

A. Defect Sensor Evaluation

The effectiveness of the Defect Sensor in detecting resistive-open and resistive-bridge defects has been computed considering the scheme presented in Fig. 1 and Fig. 2. The defect sizes adopted during simulations varied from 100Ohm to 10MOhm in steps of 10%. Note that a weak resistive-open defect has a small resistance value, while a weak resistive-bridge defect has a big resistance value. Table I summarizes the results obtained simulating only one SRAM cell with all possible defects, one at a time. Observing Table I it is possible to see the minimum and maximum defect size detected by the Defect Sensor. Note that for the resistive-open Df1, the minimum resistance value detected by the Defect Sensor was different from the other resistive-open defects, being of 4.3kOhm. However, for resistive-bridge defects, the maximum resistance of Df5 detected by the Defect Sensor was of 3.7MOhm, making it the weakest defect. Thus, considering the defects associated to the ranges shown in Table I, the Defect Sensor was able to detect 100% of them. After performing simulations considering only one SRAM cell, simulations adopting a case study with a SRAM array of 8 columns have been performed.

TABLE I. Minimum and Maximum Resistance Values for each Defct.

Defects	Minimum Resistance	Maximum Resistance
Resistive-Open Defects		
Df1	4.3kOhm	10MOhm
Df2	100Ohm	10MOhm
Df3	100Ohm	10MOhm
Df4	100Ohm	10MOhm
Df5	100Ohm	10MOhm
Df6	100Ohm	10MOhm
Resistive-Bridge Defects		
Df1	100Ohm	10MOhm
Df2	100Ohm	10MOhm
Df3	100Ohm	10MOhm
Df4	100Ohm	10MOhm
Df5	100Ohm	3.7MOhm

Table II and Table III summarize the defect type and defective column distributions during 1000 simulations. It is important to note that the Defect Sensor has been able to detect all defects considered during these 1000 simulations.

TABLE II. Defect Type Distribution.

Defects	Distribution in [%]
Resistive-Open Defects	
Df1	8.8
Df2	8.1
Df3	7.7
Df4	9.2
Df5	9.7
Df6	9.3
Resistive-Bridge Defects	
Df1	10.1
Df2	9.5
Df3	9.6
Df4	9.7
Df5	8.3

TABLE III. Defective Column Distribution.

Columns	Distribution in [%]
0	13.2
1	11.1
2	14.0
3	11.3
4	12.8
5	13.4
6	13.2
7	11.0

B. Bit-Flip Sensor Evaluation

As previously mentioned, the Bit-Flip Sensors are activated only in field after performing a test procedure in order to individuate the SRAM cells with weak defects. In more detail, the Bit-Flip Sensor is enabled per column and takes the Latch Bank's output into account, which stays turned on during both, manufacturing test as well as bit-flip detection in field. In order to evaluate the effectiveness of the Bit-Flip Sensor in terms of bit-flip detection capability, a set of simulations has been performed considering all possible resistive defects. Table IV summarizes the critical defect sizes adopted for each defect during the simulations. Note that these values represent weak defects, since they did not propagate any faulty behavior at logic level.

TABLE IV. CRITICAL DEFECT SIZE USED DURING BIT-FLIP SENSOR EVALUATION.

Defects	Resistance Value [kOhm]
Resistive-Open Defects	
Df1	9.1
Df2	7.6
Df3	7.6
Df4	0.1
Df5	807
Df6	6.9
Resistive-Bridge Defects	
Df1	503.1
Df2	501.8
Df3	502.6
Df4	501.8
Df4	16.6 (dynamic fault behavior)
Df5	188.5

Fig. 5 shows the bit-flip detection considering an SRAM cell with the resistive-bridge Df2. Observing this figure it is possible to see the occurrence of a bit-flip followed by the bit-flip detection. Note that there is a delay between occurrence and detection, this delay is considered negligible and is caused by the GND Defect Sensor OPAMP.

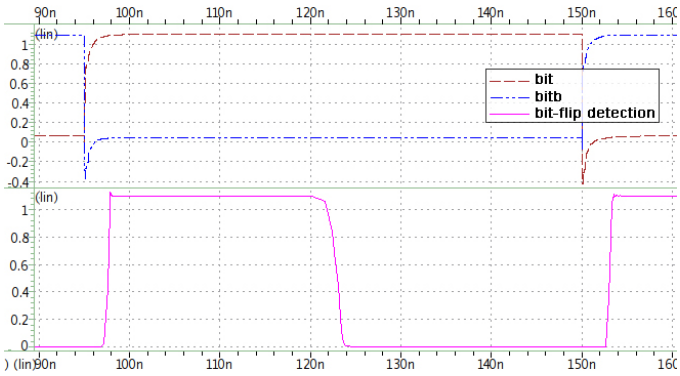

Fig. 5. Bit-flip detection considering an SRAM cell with a resistive-bridge Df2.

Fig. 6 shows the case of the resistive-bridge Df4, which represents the only case that the detection was not completely successful. Basically, the Bit-Flip Sensor was not able to detect bit-flips from "1" to "0". Observing this figure, it is possible to see two bit-flips, but only the first one is detected.

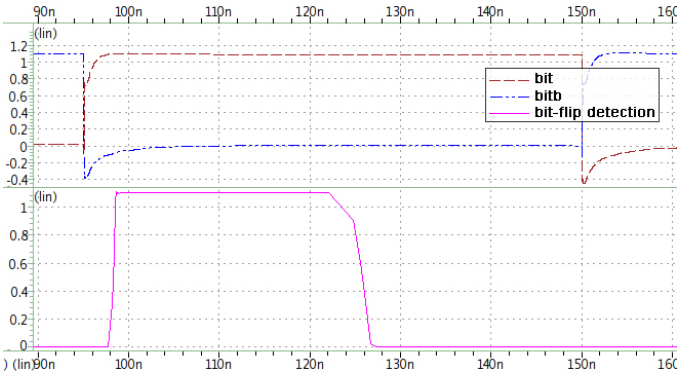

Fig. 6. Uncomplete Bit-flip detection considering an SRAM cell with the resistive-bridge Df4.

Finally, according to the performed simulations, the Bit-Flip Sensor was able to detect all bit-flips, except for the case considering a SRAM cell with the resistive-bridge Df4.

C. Overhead Analysis

In order to complete evaluation of the hardware-based approach proposed in this paper it is necessary to analyze the main introduced overheads.

Regarding timing overhead, the proposed approach needs to execute a sequence of 11 write and read operations on each cell of the SRAM row at the same time in order to identify the defective cells based on the cell's current consumption. This means that the timing overhead introduced depends on the number of rows present in the target SRAM as well as the time spent in each operation. Since the test procedure is performed just once at the memory startup and it is the only timing overhead introduced, it is possible to conclude that the proposed hardware-based approach introduces an insignificant timing overhead.

The introduced area overhead has been computed considering the sum of the transistor's area associated to the complete set of added circuits. The area estimated for each SRAM cell was of 0.0648μm^2 and the area for the proposed approach was of 8.3312μm^2. Thus, depending on the SRAM size, the area overhead becomes insignificant. In more detail, considering an SRAM of only 16kB, the introduced area overhead is already less than 1%.

Finally, the power overhead has been estimated. The power consumption related to the test procedure that has to be executed in order to individuate the SRAM cells with weak defects has not been computed, since it occurs only at the startup of the memory. However, the overhead during runtime has been measured. The power consumption estimated for an 8 per 8 SRAM without the proposed approach was 24.9μW, while for the same array with the proposed approach a consumption of 36.8μW was estimated. However, considering the same SRAM, but with 512 rows, the proposed approach incurs in an

acceptable power overhead of 1.13%, which further decreases for increasing numbers of SRAM rows.

V. Final Considerations

This paper presents a hardware-based approach able to detect resistive defects in SRAM cells during manufacturing test as well as to monitor defective cells in order to identify the occurrence of bit-flips in field. The proposed approach is justified by the fact that defects that initially did not represent a reliability problem, because they are not able to sensitize any faulty behavior and were considered as weak, may exacerbate the cell's susceptibility to SEUs. The obtained results demonstrate the effectiveness of the introduced hardware in terms of resistive defects' as well as bit-flips' detection capabilities. Furthermore, evaluation shows that the adoption of the proposed technique introduces tolerable overheads that tend to further decrease when the SRAM's size increases.

References

[1] Semiconductor Industry Association (SIA), "International Technology Roadmap for Semiconductors (ITRS)", 2005 Edition.

[2] J. C.-M. Li, C-W Tseng, E. J. McCluskey, "Testing for Resistive Opens and Stuck Opens", IEEE International Test Conference, 2001.

[3] W. Needham, C. Prunty, H. Z. Eng, "High Volume Microprocessor Test Escapes, an Analysis of Defets our Tests are Missing", IEEE International Test Conference, 1998.

[4] P. Dubey, A. Garg, S. Mahajan, Study of Read Recovery Dynamic Faults in 6T SRAMs and Method to Improve Test Time, Journal Electron Test, 2010.

[5] S. Borri, M. Hage-Hassen, L. Dilillo, P. Girard, S. Pravossoudovitch, A. Virazel, "Analysis of Dynamic Faults in Embedded-SRAMs: Implications for Memory Test", JETTA, 2003.

[6] K. Zhang, U. Bhattacharya, Z. Chen, F. Hamzaoglu, D. Murray, N. Vallepalli, Y. Wang, B. Zheng, M. Bohr, "SRAM Design on 65-nm CMOS Technology With Dynamic Sleep Transistor for Leakage Reduction", IEEE Journal of Solid-State Circuits, Vol. 40, N. 4, April 2005.

[7] D. Boning, S. Nassif, "Models of Process Variations in Device and Interconnect", Design of High Performance Microprocessor Circuits, IEEE Press, 2000.

[8] S. Borkar, "Designing Reliable Systems from Unreliable Components: The Challenges of Transistor Variability and Degradation", IEEE Micro. 25, 6, 10–16, 2005.

[9] A. Alam, "Reliability- and Process-Variation Aware Design of Integrated Circuits", Microelectronics Reliability, Vol. 48, Issues 8-9, pp. 1114–1122, Aug-Sept 2008.

[10] L. Dilillo, P. Girard, S. Pravossoudovitch, A. Virazel, "Analysis and Test of Resistive-Open Defects in SRAM Pre-Charge Circuits", Journal of Electronic Test: Theory and Applications, 2005.

[11] A. Bosio, et al., "Advanced Test Methods for SRAMs", Springer Science+Business Media, LLC 2010.

[12] H. V. Minaya, "Reliability Enhancement of Nanometer-Scale Digital Circuits", Thesis (PhD in Electrical Engineering) - National Institute for Astrophysics, Optics and Electronics. Tonantzintla, Puebla, Mexico. May 2014.

[13] R. A. Fonseca, L. Dilillo, A. Bosio, P. Girard, S. Pravossoudovitch, A. Virazel, N. Badereddine, "Analysis of resistive-bridging defects in SRAM core-cells: A comparative study from 90nm down to 40nm technology nodes", Test Symposium (ETS), 2010 15th IEEE European , vol., no., pp.132,137. 24-28 May 2010.

[14] A. F. Gomez, F. Lavratti, G. Medeiros, M. Sartori, L. Bolzani Poehls V. Champac, F. Vargas, "Effectiveness of a hardware-based approach to detect resistive-open defects in SRAM cells under process variations", Microelectronics and Reliability, v. 67, p. 150-158, 2016.