Analysis of COTS FPGA SEU-Sensitivity to Combined Effects of Conducted-EMI and TID

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***Abstract*— The desirable use of Field-Programmable Gate Arrays (FGPAs) in aerospace & defense field has become a general consensus among IC and embedded system designers. Radiation-hardened (rad-hard) electronics used in this domain is regulated under severe and complex political and commercial treaties. In order to refrain from these undesired political and commercial barriers component-off-the-shelf (COTS) FPGAs (despite the fact of their low reliability) have been considered as a promising alternative to replace rad-hard ICs. In this scenario, this paper analyses the Single-Event Upset (SEU) sensitivity of the Microsemi ProASIC3E A3PE1500 COTS FPGA for a combined set of Electromagnetic Interference (EMI) and Total-Ionizing Dose (TID) tests. This component is under pre-qualification process for use in some satellites of the Brazilian Space Program. Experimental results are herein briefly presented and discussed. These results allow us to consider this component as a strong candidate to replace rad-hard FPGAs, if its use is combined with strict system-level fault-tolerant strategies for error detection and correction (EDAC).**

Keywords*— *FPGA; SEU Sensitivity; Microsemi ProAsic3E; COTS; Combined Qualification Test for EMI; SEU and TID

I. Introduction

Although the use of Field Programmable Gate Arrays (FPGAs) has become recurrent in commercial applications, its usage is avoided in space. As the space environment is much more aggressive than the ground-based one in terms of cosmic radiation and system recovering from failure is much more difficult (if not impossible), the use of FPGAs for such purpose faces severe criticism from the scientific community. Nonetheless, we observe an increasingly adoption of FPGAs in a large number of missions [1–4], since they fill several requirements for these projects, but always taking into account the fault tolerance due to the great influence of radiation and its effects in integrated circuits [5, 6].

However, the vast majority of FPGAs used in space missions are radiation hardened (rad-hard) and not component-off-the-shelf (COTS) devices. One of the most challenging issues faced by design engineers is the possibility to implement fault-tolerant systems with COTS components. Given the Brazil's National Institute for Space Research (INPE) interest in migrating from the ERC32 (a discontinued radiation-tolerant SPARC V7 processor developed for space applications) [7] and not having to redesign the whole code from scratch, the soft-core LEON3 (SPARC V8 based) processor implemented with a COTS FPGA rises as a promising option. With this purpose, INPE has selected the ProASIC3E A3PE1500 FPGA. However, before using such FPGA in the INPE's satellite electronics, this component has to be qualified for operation in radiation (Single-Event Upset: SEU and total-ionizing dose: TID) [12] and electromagnetic interference (EMI) environments [13].

Moreover, it is worth noting that due to the high complexity required to simultaneously perform qualification test for EMI and radiation (SEU and TID), this task has been treated as an independent, fragmented event. In more detail, engineers qualify electronic systems to EMI, TID and SEU, but not considering the combined effects one phenomenon may take over the other. International standards and referred literature address only radiation (SEU + TID) qualification tests, but not taking into account the reliability degradation effects provoked by EMI and vice-versa (i.e., the system is qualified for EMI, but not taking into account the effects of SEU and TID on the EMI sensitivity of the electronics. In this context, we have recently published a first work addressing this problem, where we qualified a Xilinx Spartan3E FPGA to the combined effects of EMI, SEU and TID [9]. At present, there is only a draft standard devoted to the combined (SEU + TID + EMI) test for telecommunication electronics [11].

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In this scenario, the goal of this paper is twofold:

a) Analyze the SEU tolerance of the Microsemi ProASIC3E A3PE1500 COTS FPGA when exposed simultaneously to the effects of EMI and TID;

b) Demonstrate by experimental results the importance of performing combined tests for EMI, SEU and TID.

II. Methodology Description

The ProASIC3E A3PE1500 FPGA is cost-optimized: reprogrammable and nonvolatile. It is based on flash technology to store configuration bits, whereas volatile memory (in the form of FFs and SRAM cells) is used to store user data [10]. Some other A3PE1500 device important characteristics for safe, critical applications are: (a) it supports 128-bit AES decryption for device configuration, (b) it is single chip and live at power-up and (c) 1,024 bits of user flash memory. In order to properly perform radiation (SEU and TID) test according to the MIL-STD 883H Methods 1032.1 and 1019.8 [12], the FPGA package was opened by means of a chemical/mechanical process. Fig.1 shows the final state of the open-cavity die.

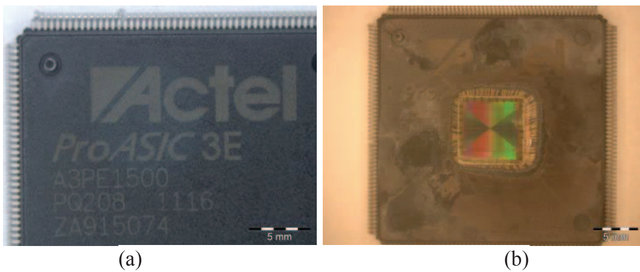


Fig. 1. Microsemi ProAsic3E A3PE1500 FPGA: (a) Packaged device; (b) Unpacked, ready for radiation (SEU and TID) tests.

The FPGA was configured with a dedicated logic written in VHSIC Hardware Description Language (VHDL) that mapped Flip-flops (FFs) and SRAM cells as a single array of memory elements that were serially accessed (First-In-First-Out, FIFO). The FFs and SRAM cells were mapped with two specific patterns: all 0's and all 1's. At the beginning of the test, all memory elements were initialized with the logical pattern "0". Then, once all measurements have been done for this pattern, all memory elements were reset and fulfilled with the logical pattern "1". These patterns were selected for two reasons:

a) to have full control of all data stored into the FPGA memory elements (FFs and SRAM cells) and

b) to observe if the FPGA sensitivity is similar for bit-flips from 0 to 1 and from 1 to 0.

Each FF and SRAM position represents an 18-bit wide structure. The used design framework was the Microsemi Libero tool. Also from Microsemi, the FlashPro tool was used to download the configuration bit-stream, as well as to read/write the FF and SRAM array via JTAG interface during the whole experiment.

The hardware configuration mapped the total allowable storage capacity of the Microsemi ProASIC3E FPGA model A3PE1500. In this case, we addressed 18,432 FFs and 276,480 SRAM bits, comprising the totality of 1,024 addresses for FFs and 15,360 addresses for SRAM cells (each address with 18-bit data wide).

Table I summarizes the ProASIC3E resource usage for the experiment and the maximum resources available for the device.

FFs are sitting in the Core Logic (named VersaTiles by Microsemi). In such logic, we occupied 18,432 FFs, which represented 48.63% of the total number of available FFs (38,400) in the FPGA. These 18,432 FFs were spread around 98.71% of the VersaTiles area and were directly accessed from the host test computer via JTAG.

TABLE I. ProASIC3E Occupied Resources

FPGA Hardware Summary	Core Logic (VersaTiles)	FFs	SRAM Cells
Used hardware configuration	37,903	18,432	276,480
Max. hardware available	38,400	38,400	276,480

The test procedure depicted in Fig. 2 was repeated 8 times, as described below:

- Step 1: Perform SEU test for the FF and SRAM array initialized with all 0's, for the fresh FPGA (no TID was deposited on the IC), with nominal VDD (no EMI noise applied on the VDD power line);
- Step 2: Perform SEU test for the FF and SRAM array initialized with all 1's, for the fresh FPGA, with nominal VDD (no EMI noise applied on the VDD power line);
- Step 3: Perform SEU test for the FF and SRAM array initialized with all 0's, for the fresh FPGA, with EMI noise applied on the VDD power line;
- Step 4: Perform SEU test for the FF and SRAM array initialized with all 1's, for the fresh FPGA, with EMI noise applied on the VDD power line;
- Repeat the previous four steps for the fresh FPGA irradiated a TID equal to 30 krad deposited on the IC.

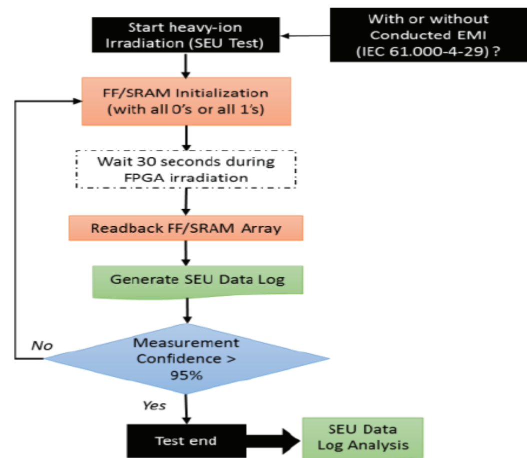
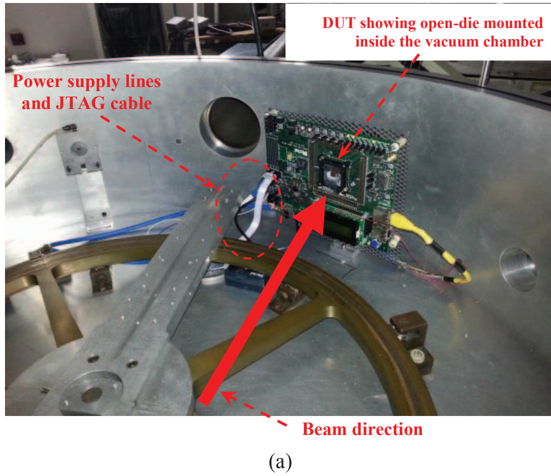


Fig. 2. Test Flow

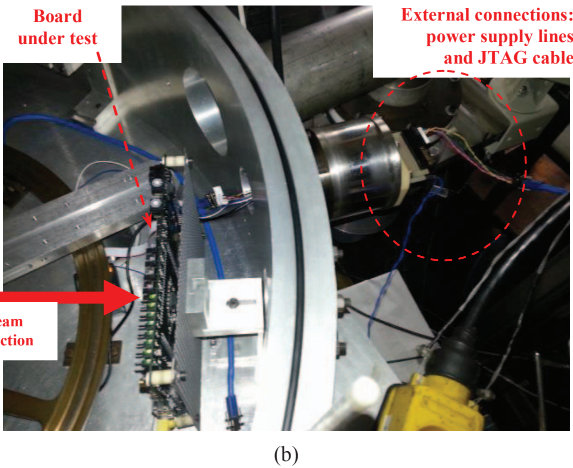
Each of the 8 test steps were repeated till we had a confidence on the measurements equal to or greater than 95%. When this amount was reached, the generated SEU datalog was analyzed.

- The SEU Test:

The Single-Event Upset (SEU) test was performed by exposing the ProASIC3E FPGA to heavy ions in an 8MV Pelletron [8] accelerator (Fig. 3 depicts the basics of the test setup). The device was irradiated with the following heavy ions: ^{16}O, ^{28}Si and ^{35}Cl.



(a)



(b)

Fig. 3. Test setup showing: (a) the device under test and the test board inside the vacuum chamber; (b) the external connections: power supply lines and JTAG cable.

- The TID test:

The total-ionizing dose test (TID) was performed by exposing the FPGA IC to a 10-keV effective energy X ray beam in a Shimadzu XRD-7000 X-ray diffractometer [15] (see Fig. 4). At the end of this experiment, we deposited a total dose of 30 krad on the device. It is worth noting that 30 krad is roughly the TID expected to be cumulated on a satellite electronics after operation for a period of 4 or 5 years in a given orbit, as specified by INPE.

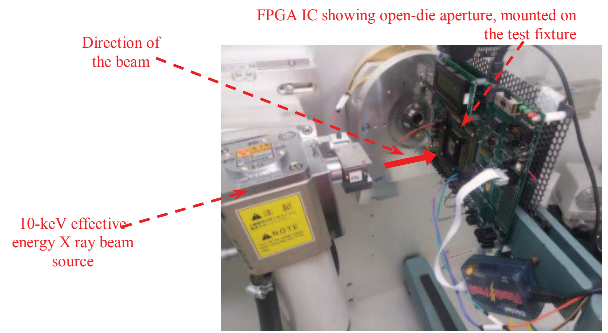


Fig. 4. 10-keV Shimadzu XRD-7000 X-ray diffractometer.

- The EMI test:

Fig. 5 depicts the noise injected in the V_{DD} power supply lines of the FPGA. Fault injection campaigns were generated according to the IEC 61000-4-29 international standard [13] by applying voltage dips to the core V_{DD} pins of the FPGA. The nominal core V_{DD} is 1.5 volts. During the experiment, the IC peripheries remained at their nominal voltage levels, i.e., 3.3, 2.5 and 1.8 volts. Voltage dips were randomly injected at the V_{DD} input pins at a frequency of 5 kHz (50% duty cycle) and consisted of dips of about 19.60% of the nominal V_{DD}. In this case, the voltage at the core V_{DD} oscillated between 1.53 and 1.23 volts. For voltage dips larger than this value, we observed the FPGA configuration loss.

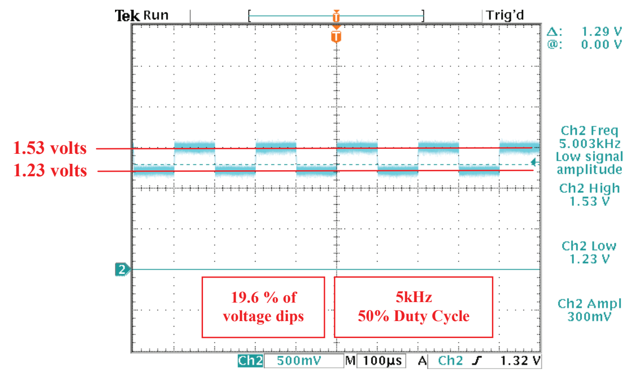


Fig. 5. Noise injected on FPGA V_{DD} pins.

III. OBTAINED RESULTS AND DISCUSSIONS

The configuration flash memory cells of the FPGA proved to be extremely robust to the set of irradiated particles (^{16}O, ^{28}Si and ^{35}Cl) and energies, since no bit-flip was observed in these structures. This conclusion is valid not only for the fresh device, but also after it was irradiated with TID (up to 30 krad). Moreover, when the conducted-EMI test was combined with SEU and TID tests, the flash memory cells presented the same robustness, i.e., no bit-flip was observed.

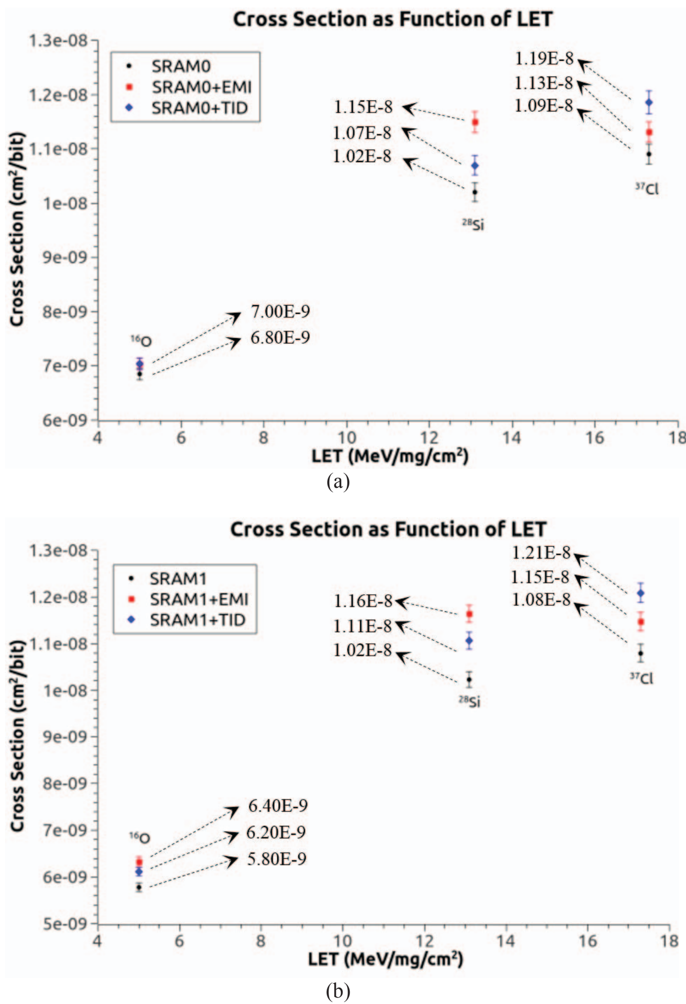


Fig.6. "Cross section versus LET" for the **SRAM cell array** of the fresh and irradiated ProASIC3E FPGA, before and after conducted-EMI noise injection: (a) SRAM cell array storing "all 0s"; (b) SRAM cell array storing "all 1s".

Cross section versus *LET* measured for the SRAM cell array of the fresh and irradiated ProASIC3E FPGA, before and after conducted-EMI noise injection is shown in Fig. 6. For those readers not familiar with this type of test, it is worth noting that as larger is the cross section of an IC, more sensitive it is to transient faults, i.e., bit-flips [14]. After meticulous analysis of the experimental data used to compose this figure, the following conclusions can be listed:

A1) The FPGA sensitivity is roughly similar when the SRAM cell array is storing "all 0s" and "all 1s": starting between 6.00E-9 and 7.00E-9 cm^2/bit up to something between 1.00E-8 and 1.20E-8 cm^2/bit. This is true no matter the device is fresh, irradiated or exposed to conducted-EMI.

B1) It is perceived that for high-energy particles (^{28}Si, ^{37}Cl), the irradiated SRAM array with 30 krad is more SEU-sensitive than the fresh one. Moreover, when the SRAM array in the fresh FPGA is exposed to conducted-EMI noise, it is more SEU-sensitive than the fresh one when operating in nominal conditions (noise-free). After analyzing log files generated during the experiments, the SRAM SEU-sensitivity increase was computed to be in the order of 5.4% for the irradiated FPGA, and 6.3% for the fresh FPGA exposed to conducted-EMI.

C1) From the numbers depicted above (B1) one can conclude that, up to the cumulated dose (30 krad), conducted-EMI noise (such as the one injected in Fig. 5, according to the IEC 6100004-29 std) is more harmful to the FPGA SRAM cells than the cumulated TID.

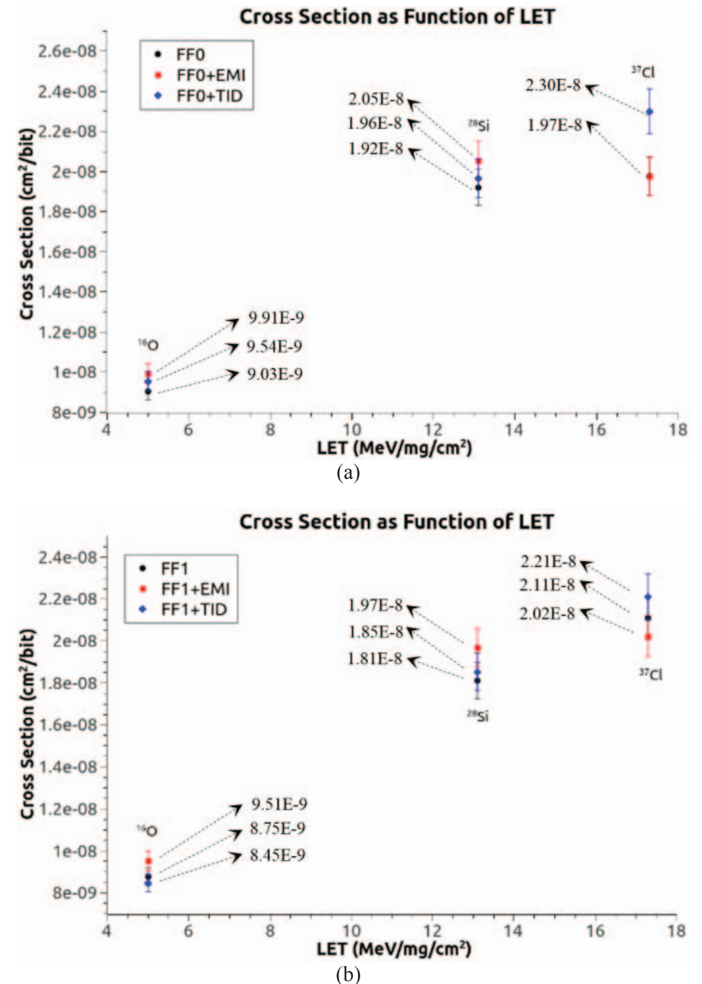


Fig. 7. "Cross section versus LET" for the **FF cell array** of the fresh and irradiated ProASIC3E FPGA, before and after conducted-EMI noise injection: (a) FF cell array storing "all 0s"; (b) FF cell array storing "all 1s".

Cross section versus *LET* measured for the FF cell array of the fresh and irradiated ProASIC3E FPGA, before and after conducted-EMI noise injection is shown in Fig. 7. After analyzing this figure, the following conclusions can be taken:

A2) The FFs are more SEU-sensitive to TID and conducted-noise than the SRAM cells, as comparing both Figs. 6 and 7. In more detail, FFs are around twice more sensitive to SEU than the SRAM cells. This is true no matter the device is fresh, irradiated or exposed to conducted-EMI. This conclusion is somehow surprising since one could expect, at a first glance, that FFs sitting in logic area should be intrinsically more robust to SEU than SRAM cells when exposed to TID or noise on power-bus.

B2) The FPGA sensitivity is roughly similar when the FF array is storing “all 0s” and “all 1s”: starting between 8.45E-9 and 9.51E-9 cm^2/bit up to something between 2.00E-8 and 2.30E-8 cm^2/bit. This is true no matter the device is fresh, irradiated or exposed to conducted-EMI.

C2) It is perceived that for high-energy particles (^{28}Si, ^{37}Cl), the irradiated FF array with 30 krad is more SEU-sensitive than the one in the fresh FPGA. Moreover, when the FF array in the fresh FPGA is exposed to conducted-EMI noise, it is more SEU-sensitive than the fresh one when operating in nominal conditions (noise-free). After analyzing log files generated during the experiments, the FF SEU-sensitivity increase was computed to be in the order of 8.1% for the irradiated FPGA, and 5.6% for the fresh FPGA exposed to conducted-EMI.

D2) From the numbers depicted above (C2) one can conclude that, up to the cumulated dose (30 krad), TID is more harmful to the FPGA FFs than the conducted-EMI noise. Note that this conclusion goes in opposite direction as compared to the one presented in (C1), where it was observed that SRAM cells SEU-sensitivity was mostly degraded by conducted-EMI noise (~6.3%) instead of cumulated TID (~5.4%).

In this scenario, if an engineer intends to design an EMI-robust embedded system for space applications, for instance, he/she should prioritize mapping relevant (critical) information to SRAM cells instead of FFs because of the following reason: even though FFs present a lower SEU-immunity degradation when exposed to conducted-EMI (5.6%) than SRAM cells (resp. 6.3%), the latter memory elements are intrinsically more robust to EMI since they present a lower cross section, in the order of almost two times lower than FFs as seem in Figs. 6 and 7. In these figures, cross section hangs from 5.80E-9 to 1.21E-8 for SRAM cells (Fig. 6, average cross-section = 0.895E-8) and 8.45E-9 to 2.30E-8 for FFs (Fig. 7, average cross-section = 1.5725E-8).

Table II summarizes the experiment results. The rightmost column indicates the results measured for the combined conducted-EMI and deposited TID over the FPGA with respect to the fresh IC. As observed, one may conclude the need to perform combined experiments for “SEU + EMI + TID” to obtain the real figure of memory elements robustness to single-event upsets. Note that the SEU sensitiveness for both memory elements (SRAM and FF) is greater for “EMI + TID” (10.8 and 9.3) than the one for the individual measurements, only for “EMI” (6.3 and 5.6) and only for “TID” (5.4 and 8.1).

TABLE II. EXPERIMENTS SUMMARY: SEU SENSITIVENESS WITH RESPECT TO THE FRESH FPGA OPERATING AT NOMINAL VDD (WITHOUT NOISE ON POWER SUPPLY LINE)

Memory Elements (average for storing 0’s and 1’s)	Experiment (%)		
	EMI	TID	EMI + TID
SRAM	6.3	5.4	10,8
FF	5.6	8.1	9,3

IV. FINAL DISCUSSIONS AND CONCLUSIONS

Component-off-the-shelf (COTS) FPGAs (despite the fact of their low reliability) have been considered as a promising alternative to replace radiation-hardened ICs. The selected FPGA was one of the most used COTS FPGAs for aerospace applications: the Microsemi FPGA ProASIC3E A3PE1500. This component is under pre-qualification process for use in some satellites of the Brazilian Space Program.

In this scenario, through this paper we:

a) Analyzed the SEU tolerance of the ProASIC3E component when exposed individually to the effects of conducted-EMI noise and total-ionizing dose (TID), as well as when simultaneously exposed to the combined effects of these two threats.

b) Demonstrated by experimental results the importance of performing combined tests for EMI + SEU + TID.

One of the important conclusions is that if an engineer intends to design an EMI-robust embedded system for space application, for instance, he/she should prioritize mapping relevant (critical) information to SRAM cells instead of FFs of the ProASIC3E FPGA because of the following reason:

- Even though FFs present a lower SEU-immunity degradation when exposed to conducted-EMI (5.6%) than SRAM cells (resp. 6.3%), the latter memory elements are intrinsically more robust to EMI since they present a lower cross section, in the order of almost two times lower than FFs.

We hope that this important conclusion can be of some support to guide engineers working on the design of robust, fault-tolerant systems based on the Microsemi ProASIC3E A3PE1500 COTS FPGA.

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