Estimation Methods for Static Noise Margins in CMOS Subthreshold Logic Circuits

Felipe T. Bortolon
UFRGS - Porto Alegre, Brazil
ftbortolon@inf.ufrgs.br

Matheus T. Moreira
PUCRS - Porto Alegre, Brazil
matheus.moreira@pucrs.br

Fernando G. Moraes
PUCRS - Porto Alegre, Brazil
fernando.moraes@pucrs.br

Sergio Bampi
UFRGS - Porto Alegre, Brazil
bampi@inf.ufrgs.br

ABSTRACT

Operating CMOS circuits at subthreshold supply voltages is an attractive solution for substantial energy reduction, at the expense of strong timing performance degradation, for a broad range of battery operated appliances. One of the challenges of this approach in current technology nodes is the reduced available noise margin when operating at low supplies. This paper evaluates the Static Noise Margin (SNM) to ensure reliable estimations in subthreshold CMOS circuits. The evaluation starts with a DC simulation of cells, providing a guideline on how its inputs should be stressed. The analysis shows that improperly employing the DC simulation may lead up to 70% worst results, thereby underestimating the SNM. The DC simulation methodology was applied herein to three different techniques, to identify which can reduce the SNM pessimism without overestimating. To extended the range of assessment, and to allow more accurate results, Monte Carlo simulations are used to evaluate the impact of both process and temperature variations on SNM for 15 different pairs (combinations) of CMOS logic cells. Results suggest that the maximum-square technique to define SNM is the most suitable for CMOS logic circuit operating in subthreshold. Those methods are validated through extensive simulation experiments with cells in a 65-nm CMOS bulk technology.

CCS CONCEPTS

•**Computing methodologies** →*Simulation evaluation;*

KEYWORDS

Static Noise Margin, Subthreshold, CMOS, combinational logic

ACM Reference format:
Felipe T. Bortolon, Matheus T. Moreira, Fernando G. Moraes, and Sergio Bampi. 2017. Estimation Methods for Static Noise Margins in CMOS Subthreshold Logic Circuits. In *Proceedings of SBCCI '17, Fortaleza - Ceará , Brazil, August 28-September 01, 2017,* 6 pages.
DOI: 10.1145/3109984.3109998

SBCCI '17, Fortaleza - Ceará , Brazil

DOI: 10.1145/3109984.3109998

1 INTRODUCTION

The increasing demand for portable applications and autonomous systems shifted system design strategy to prioritize energy consumption instead of performance [4]. At the circuit design level, a widely adopted approach is to simply reduce the supply voltage to lower values, i.e. subthreshold region. This is a very efficient technique because the dynamic power dissipation in an integrated circuit is quadratically proportional to the supply voltage. Nevertheless, scaling the voltage of the power supply has a negative impact on available noise margin, thus making digital logic circuits more sensitive to noise. Wire interconnect minimization also plays an important role on noise margin. This is because the delay of wires is now comparable to the delay of gates, and interconnect noise impact on signal characteristics and system performance became significant [7].

Given this scenario, it is important to consider noise margin when designing *combinational cells* to operate in the subthreshold region. A simple method to assess the noise tolerance of circuits is to evaluate its static noise margin (SNM), which is a technique widely used to design SRAM memories. Although this approach has been explored to design *classical CMOS gates* [2, 3, 8], the best methodology to extract the data and estimate the SNM has not received enough attention yet. In fact, there are different ways to estimate noise tolerance besides SNM, such as Dynamic Noise Margin (DNM). Each of them can rely on different methodologies and offer distinct benefits and drawbacks. While SNM is more simple to employ than DNM, its results are considered very pessimistic [11]. Therefore, it is important to analyze SNM different methodologies to reduce this pessimism and thus avoid conservative/unnecessary optimizations.

This paper assesses the impact on SNM estimates of both the DC simulation setup and the selected methodology (technique). Based on the results, the paper suggests an approach that avoids increasing by 70% SNM pessimism due to the DC simulation and a technique that allows to reduce up to 20% pessimism. For higher precision at subthreshold, the technique comparison accounts for temperature, mismatch, and corner variations through Monte Carlo analysis for 15 different cell pairs using ST 65 nm CMOS technology.

The remaining of this paper is organized as follows. Section 2 reviews the three static noise margin techniques used throughout the paper. The discussion about DC simulation setup and the suggested strategy to reduce SNM pessimism follows in Section 3. Afterward, Section 4 compares previously presented SNM techniques, presents the normal and Monte Carlo results and discusses

each one separately. Finally, Section 5 presents concluding remarks and summarizes results.

2 SNM ESTIMATION TECHNIQUES

Hill et al. [6] appears to be one of the first detailed publications regarding a logic gate voltage transfer characteristic (VTC) curve relationship with its noise margin. Succeeding his work came different approaches to calculate static noise margins that were not thoroughly discussed until 1993 by Hauser [5]. His work provides an analytical formulation about the boundaries of available techniques and demonstrates that some conventional techniques are not suited for SNM estimation. This section reviews the techniques presented in his paper that are also adopted in the current work.

2.1 Negative Slope Criteria (NSC)

One of the most simplistic approaches, the NSC estimates noise margin by identifying the two critical points of a gate VTC where its gain is unity, i.e. $\partial V_{out}/\partial V_{in} = -1$ [9]. The points that satisfy this condition are called as V_{IH}, which denotes the lowest input voltage that gets safely interpreted as a 1, and V_{IL}, which represents the highest voltage that gets recognized as 0. Associated with those points, V_{OH} indicate the lowest output voltage produced by a circuit when driving a logical 1 and, analogously, V_{OL} the uppermost voltage when at logical 0. From those definitions two possible noise margin arise: high ($NM_H = V_{OH} - V_{IH}$) and low ($NM_L = V_{IL} - V_{OL}$) noise margins. The lesser of those defines the maximum noise that can be safely admitted without compromising the circuit correct behavior ($NM = min(NM_H, NM_L)$).

2.2 Maximum Equals Criteria (MEC)

Hill [6] developed the original idea of using butterfly curves to estimate SNM and Seevinck [10] demonstrated the simulation technique to generate such curves, specifically for SRAM cells. This method plots two VTCs, as depicted in Figure 1, where one has its axis mirrored in relation to the other. From these curves, MEC defines SNM as the largest square that fits in the smaller of the wings (solid square in Figure 1). In this technique high and low noise margins are equal, and thus it is referred as Maximum Equals Criteria (MEC).

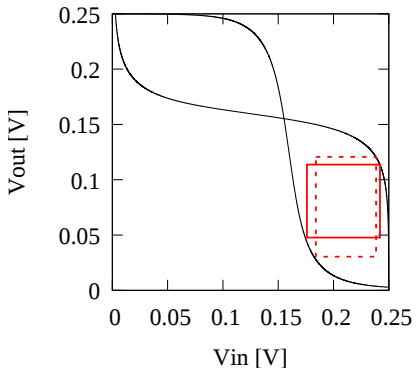


Figure 1: Maximum Equal Criteria (solid line) and Maximum Product Criteria (dashed lines) examples.

2.3 Maximum Product Criteria (MPC)

In his work, Hauser [5] proposes the Maximum Product Criteria which, similarly to the MEC, uses the butterfly curves. Nonetheless, instead of imposing equal low and high noise margins, this method maximizes the area of a rectangle, i.e. $max(NM_H * NM_L)$, which is depicted as dashed lines in Fig 1. According to Hauser, this approach is preferable to MEC since enforcing equal high and low noise margin appears to be too restrictive. In Section 4 our paper will demonstrate through a case study that this might not always be the case.

3 DC ANALYSIS FOR SUBTHRESHOLD CMOS LOGIC

The generation of an inverter VTC characteristics (V_{in} - V_{out}) is straightforward, as this gate has only one input. However, for logic circuits with more inputs or even multi-outputs, it is not clear how many (Section 3.1) and which (Section 3.2) inputs should be stimulated to evaluate the SNM of the circuit. Regarding simple digital CMOS NAND and NOR gates with multiple inputs, the derivations presented in this Section provide the following insights:

- Simultaneously switching multiple inputs generates overly conservative static noise margin estimates.
- When switching only one input, the one closest to the output terminal yields the worst-case SNM.

3.1 Number of Inputs

The techniques presented in Section 2 require a V_{in} - V_{out} transfer characteristic, similar to that VTC of an inverter, to estimate noise margins for high and low logic values. Therefore, a logic gate with multiple inputs must either simultaneously switch all inputs, or have some of them fixed to a non logic masking value (a voltage level that does not alone determine the logic gate output). A NAND, for example, cannot have inputs fixed to 0 V; otherwise, the output will stay at V_{DD}, regardless of any switching at other inputs. This condition guarantees that the logic gate behaves as a simple inverter, nonetheless with added series/parallel resistance. Consequently, it is possible to evaluate how the number of stressed inputs affects the VTC curve and thus the SNM.

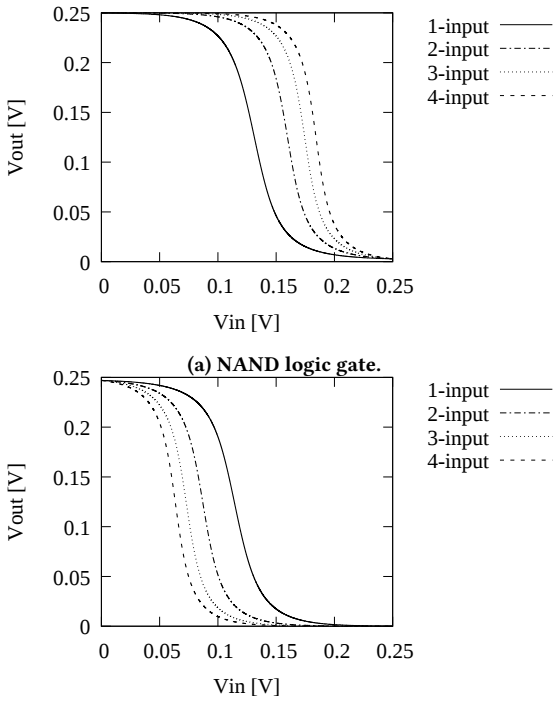
Figure 2 demonstrates how the VTC of a NAND4 and a NOR4 behaves as the number of switched inputs in the DC analysis increases. Observe that each gate deteriorates the logic level controlled by the stacked transistors, which represents the low (high) logic level for the NAND (NOR) gate. Since capacitive or inductively gate loadings are neglected in DC simulations, this variation is a function of the channel/gate resistance. Hence, to understand how this figure scales, consider the NAND4 schematic depicted in Figure 3 and the general expressions for the pull-up (R_p) and pull-down (R_n) resistances.

$$R_p = R_{A_p} \parallel R_{B_p} \parallel R_{C_p} \parallel R_{D_p} \quad (1)$$

$$R_n = R_{A_n} + R_{B_n} + R_{C_n} + R_{D_n} \quad (2)$$

where R_{G_X} represents the resistance of transistor of type X with its gate input connected to G.

Assuming only input D switching, transistor gates A, B and C are set to V_{DD} while D varies from V_{SS} to V_{DD}. With this configuration, PMOS transistors A, B and C are in cut-off (high resistivity,



(a) NAND logic gate.

(b) NOR logic gate.

Figure 2: V_{in} - V_{out} waveforms for digital CMOS (a) NAND and (b) NOR gates varying the number of simultaneously switched inputs in the DC simulation. Supply voltage of 250 mV.

R_{max}) and the equivalent NMOS transistors are in the linear region (low resistivity, R_{min}). Both D controlled transistors have their resistance dependent on V_{GS} but PMOS will transition from R_{min} to R_{max}, i.e. transistor channel begins open and ends closed, while NMOS will behave inversely. Given that $R_{max} >> R_{min}$ for digital circuits, Eqs. (1) and (2) simplify to:

$$R_{p1} = \begin{cases} (\frac{R_{max}}{3} \parallel R_{min}) \approx R_{min} & \text{for } V_{in} = V_{SS} \\ \frac{R_{max}}{4} & \text{for } V_{in} = V_{DD} \end{cases} \quad (3)$$

$$R_{n1} = \begin{cases} 3R_{min} + R_{max} \approx R_{max} & \text{for } V_{in} = V_{SS} \\ 4R_{min} & \text{for } V_{in} = V_{DD} \end{cases} \quad (4)$$

If all four inputs switch simultaneously, all PMOS begin with minimum resistance (conducting) while NMOS with maximum resistance (cut-off). Accordingly, Eqs. (1) and (2) simplify to:

$$R_{p4} = \begin{cases} \frac{R_{min}}{4} & \text{for } V_{in} = V_{SS} \\ \frac{R_{max}}{4} & \text{for } V_{in} = V_{DD} \end{cases} \quad (5)$$

$$R_{n4} = \begin{cases} 4R_{max} & \text{for } V_{in} = V_{SS} \\ 4R_{min} & \text{for } V_{in} = V_{DD} \end{cases} \quad (6)$$

Comparing equations for one (R_{p1} and R_{n1}) and for four inputs (R_{p4} and R_{n4}), it is possible to conclude that both systems finish at the same state, i.e. $V_{in} = V_{DD}$, which is expected. Nonetheless, the

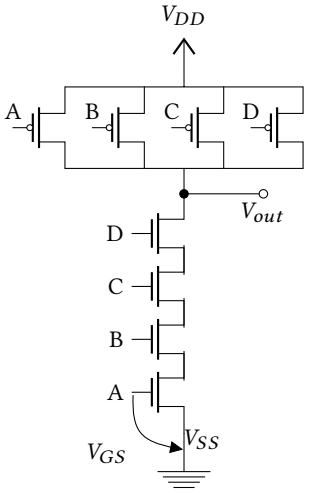


Figure 3: Electrical schematic of a 4-input digital CMOS NAND gate.

starting point, i.e. $V_{in} = V_{SS}$, of the four input case has much lower (higher) pull-up (pull-down) resistance. Hence, since transistor resistance is proportional to V_{GS}, the four input case will have overall lower pull-up resistance and higher pull-down resistance making it necessary to apply significant more input voltage to transition from logical one to zero. As V_{in} increases, both systems will converge.

This shift on the VTC curve produces significant impact on the static noise margin analysis. With the *maximum-square* method [6], for example, the noise margin estimate for a NAND4 - NOR4 gate decreases 68% from the one input to the four input DC analysis, as can be seen through the square reduction depicted in Figure 4. As the number of stacked transistor reduces (Table 1), the variation between using all (S_a) and only one (S_o) input(s) decreases ($\Delta SNM = (S_o - S_a)/S_o$), but it still is significant. Given that SNM measurements already provide pessimistic estimates [11], using more than one input further degrades this metric. Additionally, multiple inputs will rarely transition simultaneously and such analysis would implement a conservative approach to evaluate noise tolerance.

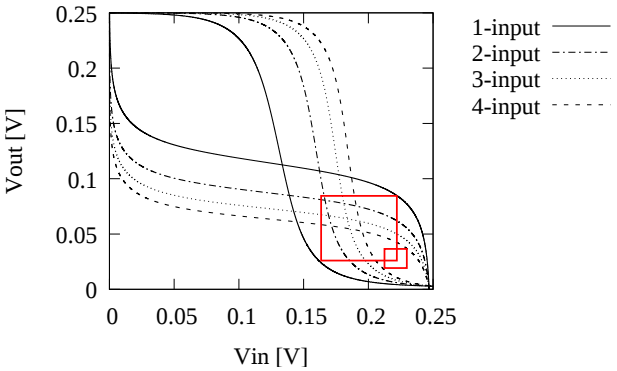


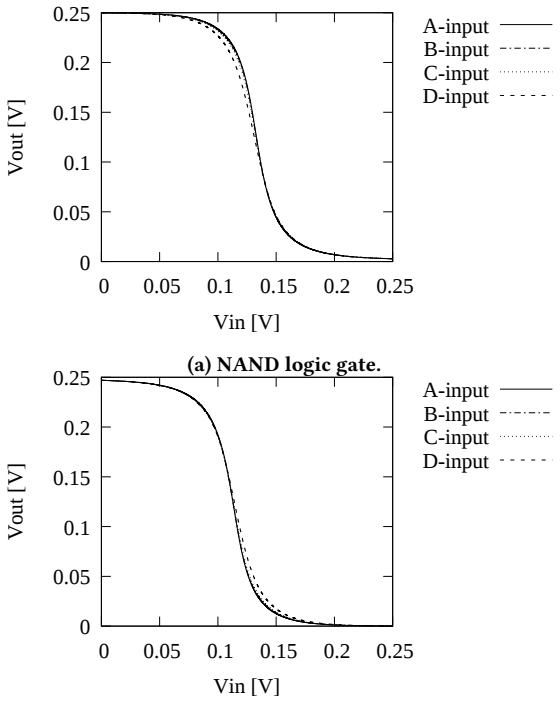
Figure 4: Relationship of NAND4 - NOR4 butterfly wing size with the number of inputs switched simultaneously.

Table 1: ΔSNM for different cell pairs, varying the number of inputs switching simultaneously (1 and 4).

Cell Pair	ΔSNM
NAND4-NOR4	68.53%
NAND3-NOR3	53.10%
NAND2-NOR2	33.06%
NAND4-NAND4	20.50%
NOR4-NOR4	22.75%

3.2 Input Location on the Stack

Based on the previous conclusion, this Section analyzes how the input location, related to the stack of transistors, affects the SNM. Considering the same NAND4 and NOR4 logic gates, Figure 5 demonstrates that despite the number of inputs switching simultaneously the produced waveforms is very similar. Hence, the SNM estimate yield only a 2% difference, using the *maximum-square* method for the NAND4-NOR4, as depicted in Figure 6. Again, let's analyze the NAND4 schematic of Figure 3 to evaluate these results.



(a) NAND logic gate.

(b) NOR logic gate.

Figure 5: V_{in} - V_{out} waveforms for NAND (a) and NOR (b) gates using only one input at a time but varying its location on the stack. DC simulation at 250 mV.

Assuming only input D (closest to the output) switching, NMOS transistors A, B and C have their $V_{GS} = V_{DD}$, and thus will be in the on state. On the opposite case, when switching input A, NMOS transistors B, C and D do not possess any connection to the ground rail and, consequently, do not begin at the on state. It is possible to perceive that the latter will slightly transition afterwards, as depicted in Figure 5 because its fixed NMOS transistors rely on transistor A to start conducting while in the other case, fixed input transistors are always conducting.

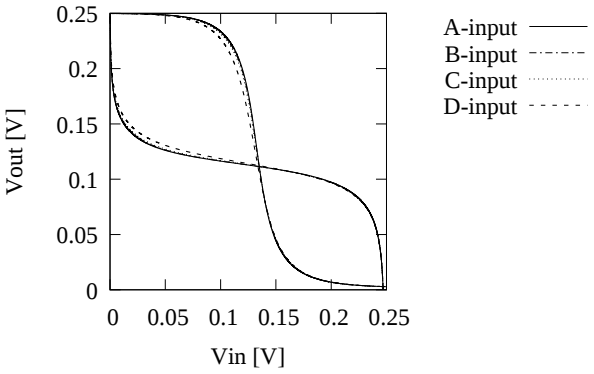


Figure 6: Relationship of NAND4 - NOR4 butterfly wing size with the selected input in the DC analysis.

To further illustrate this statement, consider Alioto et al. [1] transistor modelling for subthreshold operation. In his analysis the MOS transistor is either represented by a current-source when $V_{DS} \gg v_t$ (Eq. (7)) or by an equivalent resistor when $V_{DS} \ll v_t$ (Eq. (8)).

$$I \approx \beta \cdot e^{\frac{V_{GS}}{nv_t}} \qquad \text{for} \quad V_{DS} \gg v_t \tag{7}$$

$$R_{eq} = \frac{v_t}{\beta e^{\frac{V_{GS}}{nv_t}}} \qquad \text{for} \quad V_{DS} \ll v_t \tag{8}$$

$$\beta = I_0 \frac{W}{L} e^{-\frac{V_{TH0} - \lambda_{BS} V_{BS}}{nv_t}} \tag{9}$$

where: I_0 and n are technology-dependent parameters, $v_t = kT/q$ is the thermal voltage, W/L is the transistor aspect ratio, V_{TH0} is the threshold voltage, and V_{GS} (V_{DS}) is the gate-source (drain-source) voltage.

Based on those equations, for both presented cases, NMOS transistors are initially represented by Eq. (8), which states that V_{GS} is inversely proportional to the resistance. When input D is used, other transistors exhibit small resistance because $V_{GS} = V_{DD}$, while, when input A is used, resistance is high since there is not connection to V_{SS}, i.e. $V_{GS} \approx 0\ V$. Accordingly, resistance in the first case will be lower than in the second until it approximately reaches V_{LT} (Eq. (10)) [1]

$$V_{LT} \approx \frac{V_{DD}}{2} + \frac{1}{2} n v_t \ln\left(\frac{\beta_p}{\beta_n}\right) \tag{10}$$

where: V_{LT} is the logic threshold voltage.

Observe that V_{LT} does not depend on V_{GS} and thus should be approximately the same for all cases, as it can be seen in the DC simulations of Figure 5. In conclusion, the noise margin is slightly lower when the stressed input is located next to the output terminal.

Summarizing this section, the DC analysis of a logic gate with several inputs should use a single input DC switching when estimating SNM values in order to avoid too conservative metrics. Moreover, the designer should use the input closest to the output terminal to account and extra 2% precision.

4 NOISE MARGIN TECHNIQUES

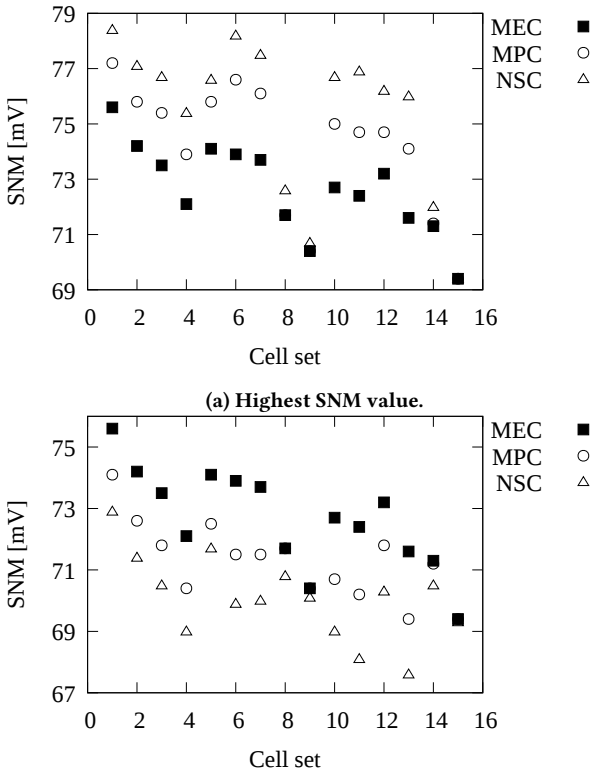
The technique choice also impacts on static noise margin estimates. Even though Hauser [5] provides a valuable discussion about the three approaches presented in Section 2, his paper did not quantitatively express their differences. Accordingly, this section aims to compare the different technique results using pairs of back to back cells described in Table 2. This is a common approach in SRAM memory cells and has also been used also to evaluate simple NAND/NOR CMOS logic gates [2, 3, 8]. The cells are described in ST 65nm CMOS bulk technology, operating at subthreshold supply voltage of 250 mV (V_{th} = 373 mV).

Table 2: MEC Monte Carlo SNM mean normalized with MPC results at 27°C.

Cell Pair	Ref.	TT	FF	SS	FS	SF
INV-INV	1	4.6%	4.4%	5.0%	18.3%	16.1%
INV-NAND2	2	4.5%	4.3%	5.0%	18.4%	16.5%
INV-NOR2	3	4.8%	4.4%	5.0%	19.1%	15.9%
NAND2-NOR2	4	4.6%	4.3%	5.0%	19.3%	16.5%
NAND2-NAND2	5	4.6%	4.4%	5.0%	18.6%	17.2%
NOR2-NOR2	6	4.1%	4.3%	5.0%	19.4%	15.8%
INV-NAND3	7	4.6%	4.4%	5.0%	18.7%	16.9%
INV-NOR3	8	3.6%	3.9%	5.0%	17.6%	18.0%
NAND3-NOR3	9	2.8%	4.5%	5.0%	18.2%	18.8%
NAND3-NAND3	10	3.2%	4.4%	5.0%	19.2%	17.8%
NOR3-NOR3	11	3.5%	4.9%	5.0%	16.5%	19.5%
NAND2-NAND3	12	4.4%	4.1%	5.0%	18.9%	17.6%
NOR2-NAND3	13	4.4%	4.1%	5.0%	19.4%	16.7%
NAND2-NOR3	14	4.0%	4.6%	5.0%	17.8%	18.5%
NOR2-NOR3	15	3.8%	4.2%	5.0%	18.4%	17.9%
Average		4.1%	4.3%	4.6%	18.5%	17.3%

4.1 Preliminary simulation

To assess the techniques prior to Monte Carlo simulation, Figure 7 depicts the SNM estimates for simple DC analysis. Since both MPC and NSC generates two values, i.e. $NM_H \neq NM_L$, the plot is sub-divided into highest (Figure 7.a) and lowest (Figure 7.b) estimates. This figure demonstrates that MEC gives a midpoint when compared to the other two and that NSC provides the highest and lowest values. Comparing both, NSC has values, on average, 3.5% higher (with a maximum of 5.9%) and 3.7% lower (with a maximum of 6.2%). Given SNM already is a pessimistic metric and that designers usually use lowest values to optimize cells, using NSC would impose extra 6.2% stricter constraints for the worst case. Moreover, using NSC highest estimates might provide too optimistic results since it is 11% larger than its lowest values.



(a) Highest SNM value.

(b) Lowest SNM value.

Figure 7: Comparison between techniques lowest (a) and highest (b) SNM estimates at 250 mV supply voltage. X-axis corresponds to the "Ref" column of Table 2.

On the other hand, MPC results are close to those of MEC, differing a maximum of 2%. Depending on the butterfly wing format, the results are even equal since, for those cases, MPC achieves maximum product when sides are approximately equal. Given those results, it is necessary to apply Monte Carlo analysis on MEC and MPC to further compare them. The NSC, however, is not further considered due to its stricter constraints. This agrees with Hauser's work [5] which says that NSC is not a reliable approach to evaluate noise margin.

4.2 Monte Carlo simulation

Subthreshold circuits rely on Monte Carlo analysis to ensure proper behavior in the presence of variations, given their sensibility to delays mismatch caused by such variations. For this reason, Table 2 depicts a comparison between MEC and MPC for TT, SS, FF, FS and SF corners operating at 250 mV at 27°C and using 1,000 Monte Carlo samples. To determine MPC data from the simulation the lowest value was chosen as this would be the usual safe approach. The table demonstrates that the *mean value* of MEC is, on average, 4.3% higher than those of MPC for TT, FF and SS corners. On FS and SF corners, MEC values are 18% higher than those of MPC. Therefore, if a designer evaluates his cell library with MPC to propose optimizations, he would adopt a strategy 18% more conservative than if he had used MEC. On the other hand, if the Monte Carlo data

for MPC technique was based on its highest estimate the designer would equally impose too relaxed constraints. For those reasons, the paper suggests that the MEC, also known as maximum-square, is a suitable technique for evaluating combinational cells at subthreshold. Furthermore, MEC does not force the designer to chose between two discrepant values and it is an approach already widely tested in SRAM memory cells.

4.3 Temperature/Corner Analysis

Considering Monte Carlo MEC mean estimates at TT corner as the baseline, moving to corner: (i) SS increases 6%, (ii) FF decreases 8.7%, (iii) F(p)S(n) decreases 14.8%, and (iv) S(p)F(n) decreases 12.7% of available noise margin. Therefore, it is possible to notice that the most stringent corners that the designer has to verify is when NMOS and PMOS transistors suffer opposite effects, i.e. FS and SF. The VTC shift in those cases sums up and the overall wings become distorted. Moreover, this behavior, which is depicted in Figure 8, demonstrates why MPC yields much lower values than MEC at these corners. To maximize the rectangle area, MPC prioritizes one dimension, e.g. y-axis, and thus yields very distinct high and low noise margins. In consequence the designer has to choose between a high and a low noise margin estimate, opposed to MEC that offers a single median value.

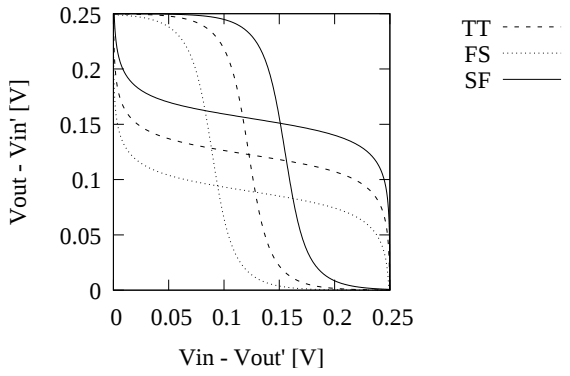


Figure 8: Corner comparison for an inverter pair at 250 mV.

Temperature also impacts on SNM estimates. As temperature increases the Monte Carlo SNM mean decreases and vice versa, as depicted in Figure 9. For a military standard, for example, it is necessary to account an extra 30% SNM reduction at its right extreme point. It is relevant to point out here that if MPC was used instead of MEC this value would be even higher, mainly at FS and SF corners. Accordingly, the technique choice has a significant impact on SNM estimation and thus must be properly chosen when using it to evaluate cell robustness.

5 CONCLUSIONS

This paper evaluated the usage of DC simulation and three techniques for calculating static noise margin of combinational cells operating at subthreshold. Experiments show that the DC simulation setup can lead to 70% more pessimistic results, which is an alarming value given that literature refers to SNM estimates as a pessimist metric. Hence, only the input closest to the output terminal

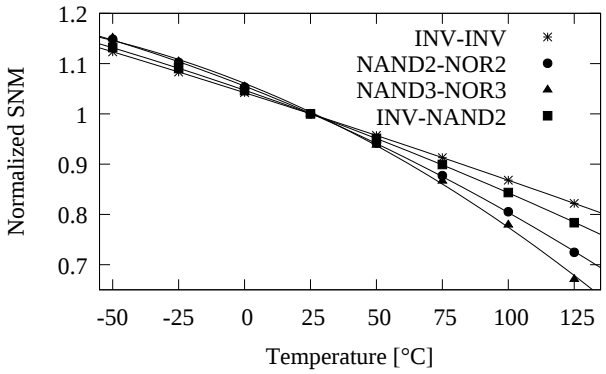


Figure 9: Monte Carlo SNM mean value versus temperature, normalized to SNM at 27°C.

should be considered to enable more realistic results, since multiple input will rarely simultaneously switch. The SNM estimation method also demonstrates a significant impact on SNM, mainly in the presence of variations, i.e. temperature, corner and process. We demonstrate that the MPC technique may lead to very pessimistic results because it prioritize one dimension, i.e either vertical or horizontal, to increase the rectangle area. This effect is accentuated on the presence of variations, which is an important analysis for subthreshold circuits. Therefore our paper suggests that the maximum-square technique can represent variation impacts without underestimating noise tolerance and thus avoid establishing a too conservative approach. Results have been validated through simulations in 65-nm CMOS bulk technology.

6 ACKNOWLEDGEMENT

The Author Fernando Gehm Moraes is supported by CNPq funding agency.

REFERENCES

[1] M. Alioto. 2010. Understanding DC Behavior of Subthreshold CMOS Logic Through Closed-Form Analysis. *IEEE Transactions on Circuits and Systems I* 57, 7 (July 2010), 1597–1607.
[2] Valeriu Beiu, Azam Beg, Walid Ibrahim, Fekri Kharbash, and Massimo Alioto. 2013. Enabling sizing for enhancing the static noise margins. In *ISQED*.
[3] Valeriu Beiu, Walid Tacheand, Mihai Ibrahim, Fekri Kharbash, and Massimo Alioto. 2013. On Upsizing Length and Noise Margins. In *Semiconductor Conference (CAS)*.
[4] Scott Hanson, Mingoo Seok, Yu-Shiang Lin, Zhiyoong Foo, Daeyon Kim, Yoonmyung Lee, Nurrachman Liu, Dennis Sylvester, and David Blaauw. 2009. A Low-Voltage Processor for Sensing Applications with Picowatt Standby Mode. In *IEEE Journal of Solid-State Circuits (JSSC)*, Vol. 44. 1145–1155.
[5] J. R. Hauser. 1993. Noise margin criteria for digital logic circuits. *IEEE Transactions on Education* 36, 4 (Nov. 1993), 363–368.
[6] C. F. Hill. 1968. Noise margin and noise immunity in logic circuits. In *Microelectronics*, Vol. 1. 16–21.
[7] Hubert Kaeslin. 2008. *Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication.* Cambridge Univ. Press, Cambridge.
[8] J. Kwong and A. Chandrakasan. 2006. Variation-Driven Device Sizing for Minimum Energy Sub-threshold Circuits. In *International Symposium on Low Power Electronics and Design*. 8–13.
[9] Jan M Rabaey, Anantha P Chandrakasan, and Borivoje Nikolić. 2007. *Digital Integrated Circuits: A Design Perspective.* Prentice-Hall.
[10] E. Seevinck, F.J. List, and J. Lohstroh. 1987. Static-noise margin analysis of MOS SRAM cells. *IEEE Journal of Solid-State Circuits* 22 (1987), 748–754. Issue 5.
[11] J. M. Zurada, Y. S. Joo, and S. V. Bell. 1989. Dynamic noise margins of MOS logic gates. In *IEEE International Symposium on Circuits and Systems*. 1153–1156 vol.2.