Evaluating a Hardware-Based Approach for Detecting Resistive-Open Defects in SRAMs

F. Lavratti, L. M. Bolzani Poehls, F. Vargas

School of Engineering

Catholic University of Rio Grande do Sul

(PUCRS)

Brazil

leticia@poehls.com

A. Calimera, E. Macii

Politecnico di Torino

Italy

Abstract—Advances in Very Deep Sub-Micron (VDSM) technology have made possible the integration of millions of transistors into a small area and consequently, has increased the circuit's density. The increase of Nano-Scale Static Random Access Memories (SRAMs) density has become an important concern for testing, since generated new types of defects that can occur during the manufacturing process. The rapidly increasing need to store more information results in the fact that the memory elements occupy great part of the System-on-Chip's (SoC) silicon area. In this context, the present paper describes and evaluates a technique based on On-Chip Current Sensors (OCCS) and Neighbourhood Comparison Logic (NCL) to detect resistive-open defects in SRAMs. Experimental results obtained throughout simulations demonstrate the technique's efficiency as well as its behaviour considering process variation. To conclude, an analysis of the overheads makes possible the comparison with today's standard techniques.

Keywords—SRAM; Resistive-Open Defects; On-Chip Current Sensor; Neighborhood Comparison Logic

I. INTRODUCTION

Technology scaling has made possible the integration of millions of transistors into a small area, allowing the increase of circuits' density. The rapidly increasing need to store more information results in the fact that the Static Random Access Memories (SRAMs) occupy great part of the System-on-Chip's (SoC) silicon area. Therefore, memory has become the main contributor to the overall SoC area. Indeed, technology scaling has led to the development of new types of defects and consequently new fault models, which differ from the traditional functional ones usually adopted by SRAM testing [1]. The latter models have become insufficient to model the effects produced by some specific defects, generated during the nanoscale manufacturing process. Consequently, testing techniques based on those models are not able to guarantee the level of reliability required for critical applications based on SoCs anymore [2].

Nowadays, resistive-open defects have become one of the most significant problems in VDSM technologies due to the presence of many interconnection layers and an ever growing number of connections between each layer [2]. A resistive-open defect is defined as a defect resistor between two circuit nodes that should be connected [3]. According to [4], Intel reports that vias are the most common root cause of test escapes in submicron technologies. Traditionally, open defects were an area of concern, which has now moved towards weak resistive-open defects. Further, the distribution of such defects is directly correlated to the number of dynamic faults [4]. This defect generally causes timing dependent faults, which means that usually a 2-pattern sequence is necessary to sensitize it [5]. According to [4], faults requiring a large number of at-speed operations on each memory cell for sensitization are denominated dynamic faults. It is important to highlight that currently used tests are mostly designed for static faults, not being able to detect dynamic faults. Most of the standard March algorithms fail to detect such dynamic faults [4][6]. It poses a significant challenge to provide the detection of dynamic faults in memory cells and consequently, to guarantee the SRAM's reliability during the lifetime.

In the last years, different techniques have been proposed in literature in order to deal with the detection of faults associated to resistive-open defects in SRAM cells. In [2], the authors demonstrated that the use of a unique March test solution can detect faults associated to resistive-open defects. Although it has been proven that a variety of March algorithms can provide efficient detection of static faults, the detection of dynamic faults is guarantied only by the adaption of a sequence of n read operations, like *1w0(r0)n*. The number of operations that is needed to detect dynamic faults related to resistive-open defects depends directly on the defect's size. Due to this fact, it is assumed to be impossible to identify an ideal value for *n*, as a low value may not arise enough stress to cause faulty behaviour and high values are causing a significant time overhead.

In this scenario, the development of new at-speed test solutions able to provide detection of dynamic faults, while guaranteeing the minimal area, time and power consumption overheads, has become essential.

This work presents a solution able to detect resistive-open defects in SRAMs using On-Chip Current Sensors (OCCSs) and Neighbourhood Comparison Logic (NCL). The main idea behind the hardware-based technique proposed is to monitor the current that flows through SRAM cells and compare the obtained value of a specific cell with its neighbouring cells to provide the detection of manufacturing defects. The proposed technique focuses on the detection of resistive-open defects, being able to detect static and dynamic faults associated to

weak resistive-open defects as well as the defects' presence, even if no fault is sensitized during the testing execution. The fault detection capability as well as the impact related to process variation of the proposed hardware-based solution has been evaluated through simulations based on a 65nm technology library of STMicroelectronics. Finally, the area, time and power consumption overheads have been estimated and the impact of process variations on this hardware-based technique have been analysed, both demonstrating its efficiency and viability.

II. MODELING RESISTIVE-OPEN DEFECTS

During manufacturing process, a standard 6-transistor SRAM cell, which is composed of four transistors that form two cross-coupled inverters and 2 nMOS transistors that provide read and write access to the cell, can be produced including resistive-open defects that can modify the correct behaviour of the memory cell. These defects can be functionally characterized according to the fault model presented in [7]. In more detail, this fault model represents the set of the following faulty behaviours:

- Transition Fault (TF): A cell is said to have a TF if it fails to undergo a transition from 0 to 1 or from 1 to 0 when it is written;

- Read Destructive Fault (RDF): A cell is said to have an RDF if a read operation performed on the cell changes the data in the cell and returns and incorrect value on the output. A dynamic RDF (dRDF) occurs if a write operation immediately followed by a read operation performed on the cell changes the logic state of this cell and returns an incorrect value on the output;

- Deceptive Read Destructive Fault (DRDF): A cell is said to have a DRDF if a read operation performed on the cell returns the correct logic value, and it changes the contents of the cell. A dynamic DRDF (dDRDF) occurs if the faulty behaviour associated to the read operation is observed immediately after a write operation.

- Incorrect Read Fault (IRF): A cell is said to have an IRF if a read operation performed on the cell returns an incorrect logic value, and the correct value is still stored in the cell.

The scheme adopted to model the previously described faults uses 6 resistors according to positions defined in [7]. Figure 1 shows the scheme of a standard six-transistor SRAM cell, where it is possible to see the resistor (Df) used to model the dRDF.

According to [7] a resistive-open defect in the pull-up of one of the core-cell inverters, as Df in Figure 1, is a classic hard-to-detect fault. More details about the behavior of dynamic faults are available in [7]. It is important to highlight that according to the resistance value, the fault behavior can be different and consequently the fault is detected by different operation sequences. According to [7] the number of read operations necessary to detect a *dRDF* is inversely proportional to the resistance value of the injected *Df*.
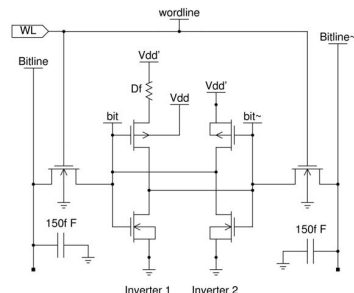

Fig. 1.   Six-transistor SRAM cell with *Df* associated to dRDF.

Thus, in order to better understand the impact of resistive-open defects, the 6 defects have been modelled. In fact, weak resistive-open defects are directly associated to dynamic faults. Observing Figure 2 it is possible to see the relation between resistance value and faulty behaviour. In more detail, it is possible to identify that depending on the resistance value, the faulty behaviour observed changes between static and dynamic. Note that the insertion of *Df4* did not generate any faulty behaviour during the performed simulations and consequently, this defect has not been included in Figure 2.
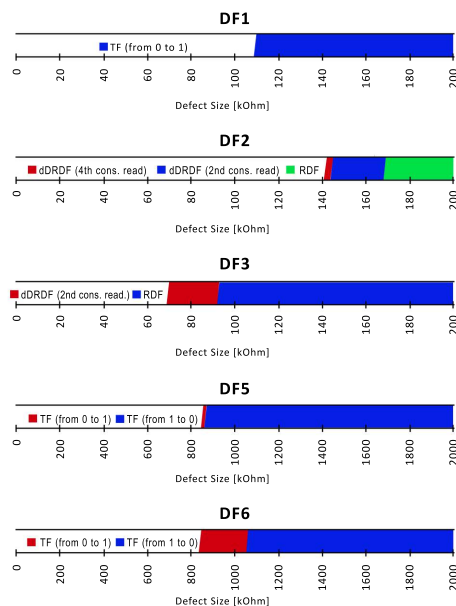

Fig. 2. Defect and faulty behavior.

It is important to highlight that resistive-open defects decrease the current that flows in the defective SRAM cell's node and consequently, causes loss of circuit's operation speed decreasing the performance of one of the inverters. Therefore, it can be defined that resistive-open defects impact the SRAM's current consumption.

Figure 3 shows the behaviour of 2 defective and 1 non-defective SRAM cell with respect to the current consumption when applying a specific sequence of write and read operations *(w1, r1, w0, r0)*. The depicted result has been achieved

inserting a resistance of 50kOhm in the position related to Df1 and Df2.

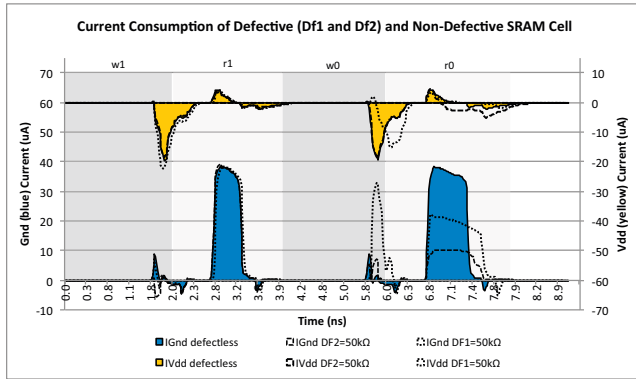Fig. 3.   Current consumption: *Gnd* current (*IGnd*) and *Vdd* current (*IVdd*) for non-defective and defective SRAM cell at 50kOhm.

Observing Figure 3 it is possible to see that the resistance value is sufficient to vary the cell's current variation, but the authors highlight, that these variations do not trigger any faulty behaviour. Further, it can be observed that resistive-open defects may cause an increased or decreased current, rendering their detection impossible, if predefined thresholds are used. Finally, it is important to note that different current consumption's distortion can be observed depending on the defect's position resulting in altered amplitudes as well as off-sets.

III.   The Hardware-Based Approach

The technique presented in this paper is able to monitor the current consumption of SRAM cells in order to provide the detection of resistive-open defects whether they cause faulty behaviour or not. Note that weak resistive-open defects are strongly related to dynamic faults and consequently represent a critical issue for SRAM manufacturing tests. In more detail, depending on the defect's size, the faulty behaviour may appear during the memory's lifetime according to the read stress level, which the SRAM cell is exposed to. Due to the fact that resistive-open defects change the current consumption of SRAM cells even if they do not cause faulty behaviour, an OCCS that tackles this challenge by comparing the current consumption of the cell under evaluation with the current of its neighbouring cells when submitted to the same operation is proposed. Considering that parallel and simultaneous read operation should ideally cause the same current consumption, independent from the value stored and read from the cell. It is important to note that the OOCS employed monitors both the *Vdd* Current (*IVdd*) and *Gnd* Current (*IGnd*) in order to achieve the detection of resistive-open defects in SRAMs. Figure 3 depicts the OCCS. .
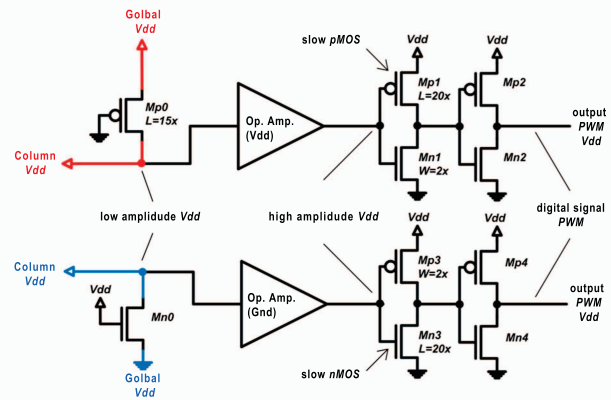

Fig. 4.   OCCS.

The OCCS is composed of the following functional blocks:

- Current-Voltage Converter: this block works as a low impedance resistor and generates a small oscillation in the *Vdd* and *Gnd* associated to SRAM columns, converting current into voltage;

- Operational Voltage Signal Amplifier (*Op. Amp.*): this block is in charge of amplifying and propagating the previously produced oscillation to the next functional block;

- Pulse Width Modulated (*PWM*) Generator: this functional block consists of two inverters in series. The first one guarantees the fast charging of the value that corresponds to the current consumption and discharges slowly, creating a time modulated analog signal. The second inverter transforms this signal into a digital signal.

Thus, the sensor acts like a 1bit Analog-to-Digital converter with a PWM output, where the amplitude and duration is represented by duration of the digital pulse. It is important to highlight that the PWM output's width is strictly related to the amplitude and duration of the current consumption of the monitored cells. However, the OCCS's output merely represents the current's behaviour and consequently leaves the identification of the defective SRAM cell to the NCL. We propose to explore the idea of using an NCL to cope with the identification of the defective SRAM cells regardless the size or position of the defect. The NCL connects the neighbouring SRAM cells in circular manner and is based on the following algorithm:

for every member N of the neighbourhood
   if (behaviour of member N == behaviour of member N+1) and
     (behaviour of member N == behaviour of Member N-1) then
      member N does not present a defect, Bit[N] exits with a value of "0";
   else
      member N can present a defect, Bit[N] exits with a value of "1";
end of loop;

For each SRAM cell *N* its behaviour is compared to its direct neighbours, *N+1* and *N-1*. The cell N is defined as "not defective" if its behaviour is similar to both its neighbours and

therefore the output bit corresponding to the cells position is set to "0". In case that a cell behaves unequal to one or both neighbours it is defined as "possibly defective" and its corresponding bit is set to "1". In order to obtain more detailed information about the position of the defective SRAM cell, while introducing little area overhead, the adopted strategy always uses neighbourhoods of four cells from different columns, but the same line. As a result the logic is implemented using 4 OR and 4 XOR logic gates only. Therefore, the de-codification of the output value follows the rules below:

- 0000/0x0h identifies no defective cell;

- 1011/0xBh identifies cell 0 as defective;

- 0111/0x7h identifies cell 1 as defective;

- 1110/0xEh identifies cell 2 as defective;

- 1101/0xDh identifies cell 3 as defective;

- 1111/0xFh identifies more than one cell as defective.

Looking at the de-codification results, we can observe that the output makes possible the identification of no, one or more than one defective SRAM cell. The NCL analyses a digital signal that represents the behaviour of cells from one neighbourhood. The PWM signal generated by the OCCS is related to the current consumption over an axis of time. As such data varies over time, it demands an advanced processing capacity to capture all the signal's information. To lower the complexity of the stage that monitors the output of the NCL blocks, one Flip-Flop (FF) was inserted at every NCL block. Thereby the signal "1" is granted preferential prorogation in time. In more detail, a signal changed to "1" remains in that state until the FF is re-initialized, and consequently the indication of a possible defect is dominant over time, which guarantees an absolute preciseness of the "not defective" information represented by "0". As mentioned before two different currents are measured in parallel, in order to achieve a single output result for each neighbourhood, the output data for corresponding *IVdd* and *IGnd* are compared using an OR logic gate. By doing so, the signal carrying a "1" propagates. Resuming, the complete technique for defect detection considering the first 8 columns of a SRAM is depicted in Figure 5.
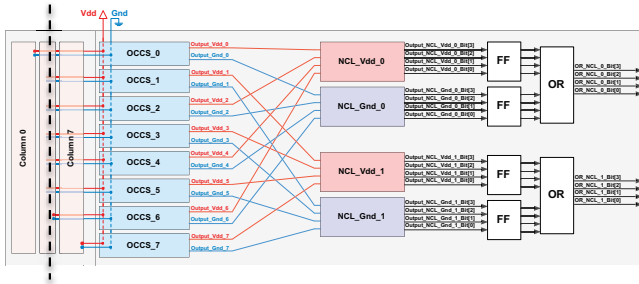

Fig. 5. Diagram representing the complete hardware-based technique composed of the OCCSs and NCL blocks.

IV. EXPERIMENTAL RESULTS

In order to evaluate the effectiveness of the hardware-based technique electrical simulations based on a SRAM, composed of 1024 lines in 8 columns, have been performed. Figure 6 demonstrates that the SRAM adopted during the evaluation of the hardware-based approach is able to tolerate inter-die process variation (FF, SS, SF, FS and TT at -40°C, 27°C and 100°C). In more detail, Figure 5 depicts the stored (bit) as well as the output value considering the previously mentioned corners. Note that the results associated to TT at 27°C are depicted in black.

The insertion of resistors is able to model the effects produced by resistive-open defects in SRAM cells. With the scope of continuity, the results presented below demonstrate the proposed technique's ability in order to detect resistive-open defects in three situations: (1) the defect's size is sufficient to characterize a static fault in SRAM cell behaviour; (2) the defect's size is not sufficient to model a static fault, but is sufficient to model a fault characterized as dynamic, since it has been detected after a limited number of read operations and (3) the defect inserted in SRAM cell is considered weak and consequently, it is not able to sensitize the faulty behaviour.
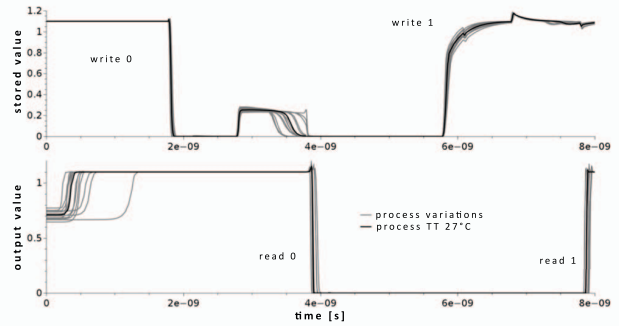

Fig. 6. Stored and output value of the adopted SRAM considering different corners.

The graphs depicted in Figure 7 demonstrate the situations previously mentioned. It is important to highlight that the authors performed simulations using a 65nm technological library by STMicroelectronics considering the corner defined as typical, with the temperature set to 27ºC and the voltage to 1.1V.

Figure 7a shows the detection of a TF modelled using a resistor of 140kOhm in the position of Df1. In more detail, this figure depicts a standard fault detection, which is based on the functional failure to be observed after a tentative to write the logic value of "1" into the SRAM cell. This occurs after about 6ns. However, it is important to note that the proposed technique is able to identify the defective cell after about 3ns. According to the de-codification, 0xEh indicates a defect in the SRAM cell associated N=2. It is important to highlight, that this type of defect, resulting in functional misbehaviour, is detected by classic fault detection methodologies, but the detection occurs only after the fault's sensitization. As laid out before the traditional fault detection techniques fail to detect weak resistive-open defects due to the fact that they only cause

functional misbehaviour when the defective cell is exited by several consecutive operations.

Figure 7b summarizes the detection of a dDRDF modelled using a resistor of 122.11kOhm in the position of Df2. Figure 7b shows an example, where the functional misbehaviour occurs after 8 read operations. With an adequate March-Algorithm this fault could be detected after about 20ns. The proposed technique is taking about 6ns to indicate that the SRAM cell (N=2) is presenting a defect. This example clearly shows, how the proposed technique enables a faster detection, in fact the technique takes only 30% of the time a fault detection algorithm would to indicate a concern.

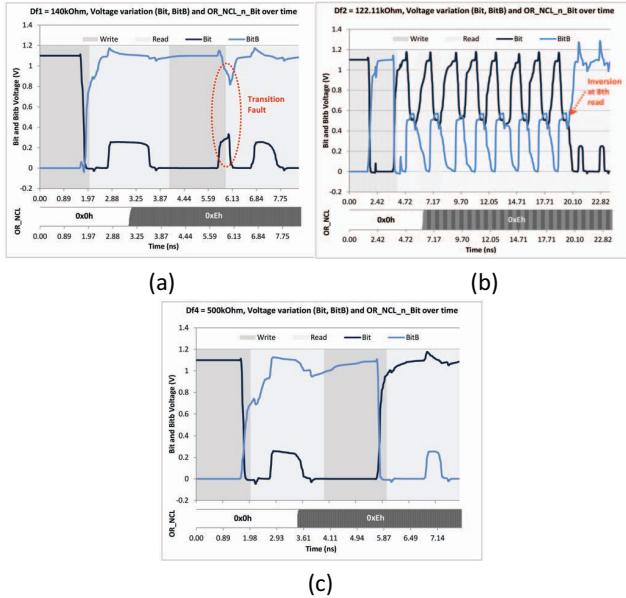(a)   (b)

(c)

Fig. 7. Detection of (a) TF, (b) Detection of dDRDF after 8 read operations, (c) Detection of weak resistive-open defects by the proposed hardware-based technique.

The last graph presented in Figure 7c shows the simulation related to the insertion of Df4 with 500kOhm. The situation shown in Figure 5c exemplifies the behaviour observed when a weak resistive-open defect is present, but no faulty behaviour is sensitized. It is important to highlight that such defective SRAM cell, due to aging effects may cause faulty behaviour in the future. Due to the fact that the proposed technique is based on current variation it is able to identify the existence of a defective cell in the SRAM after about 3ns.

In order to evaluate the impact of process variation on the OCCSs and NCL blocks, Monte Carlos simulations have been performed. In more detail, the following parameters have been varied: (1) *Def_Cell* that represents the number of defective cells in the adopted SRAM; (2) *Type_Def* that can vary from 1 to 6 and is related to the position of the inserted defect and (3) *Size_Def* that represents the size of the resistor inserted in order to model the defect. Note that the *Size_Def* can assume infinite values and in order to identify a behavioural tendency simulations have been performed. The obtained results demonstrate that OCCS's detection capability increases with the increase of *Size_Def* as well as with the decrease of

Def_Cell. In more detail, the presented technique will achieve its best detection capability (0% of test escape) when considering an SRAM with 1Gbit, a *Def_Cell* of around 1% and a *Size_Def* smaller than 5kOhm. Considering this situation, the hardware-based approach will detect all defective cells and will have less than 0.029% of false detection. Indeed, it is important to highlight that, due to its use of CMOS transistors operating in linear region, the OCCSs represent the most sensitive element. Thus, hardware-based approach supports any type of inter-chip process variation, since it works properly considering all different corners of the adopted technology library.

Regarding area overhead, the authors estimate an increase of about 5.5% considering a SRAM composed of 1024 lines in 8 columns, which means that a word is composed of 8 bits. The estimative has been done without considering the area necessary to perform the routing of the interconnections. In more detail, the hardware-based technique consumes 132 nMOS and 156 pMOS transistors equalizing an area of 3.2904µm2. In other words, the proposed technique needs to introduce the equivalent area of 56 SRAM cells for each monitored column. It is important to highlight, that considering a memory with 8224 lines in 64 columns, would result in an area overhead of only 0.68%.

An analysis of the power consumption overhead has been performed. The power consumption of the proposed technique is of about 95% of the total leakage power of a 256B at ambient temperature. As expected the introduced hardware's contribution decreases drastically for greater memories. Applying the technique's components to a 32KB SRAM, the impact on the total leakage power is to be of about 55%. The analysis shows, that higher ambient temperatures cause even more convenient proportions, at 125ºC a 32KB SRAM accounts for 85% of the power consumption, in other words, the techniques impact is of 15% only.

Finally, the number of memory accesses as well as the execution time of the presented approach have been compared with the ones related to MarchSS, MarchSD and MarchRAW. The obtained results demonstrate that the number of memory accesses required by the presented technique is of 5120, while March SS requires 180224, MarchSD 163840 and MarchRAW 212992. Regarding the execution time, the presented approach requires around 10% of the time required by the other three approaches.

V. CONCLUSIONS

The analysis of the results obtained with the proposed technique using OCCSs and NCL blocks applied to a SRAM show that the technique is not only able to detect resistive-open defects that do cause faulty behaviour faster then all known March testing techniques, but also detects defects in SRAM cells that do not sensitize any faulty behaviour. To detect weak resistive-open defects in SRAMs, the proposed technique inserts 4 NCL blocks composed of 4 bits and 8 OCCSs for each column. The OCCSs respectively monitor the *IVdd* and *IGnd* and create one digital PWM output signal for each analog signal, generating a total of 16 signals to be analysed by the proposed NCL blocks.

It is important to highlight two shortcomings of the proposed technique. Firstly, the methodology by comparison is based on the assumption that a great part of the cells in a neighbourhood will present similar currents. Secondly exists a mathematical limitation of such comparison. Given that from the total of 16 interpretations 5 are correct, 6 are imprecise and 5 are not correct. Nevertheless, it does not necessarily mean that 31% of the results will be interpreted in a way that does not correspond to the situation of the hardware of the evaluated cell. The chances that one of the two cases occurs are significantly lower. The real probability depends on the type of application run. For resistive-open defects to occur the probability that 3 or 4 cells of a neighbourhood present a similar current variation, in other words, that the same defect affects 3 or 4 cells of neighbouring positions is extremely rare.

Resuming, the proposed technique is highly adapted to resistive-open defects in SRAM cells. The area overhead is considered acceptable for the simulated SRAM and the obtained results show that the impact reduces when the memory's size increases. As the test uses a relatively small memory the introduced overhead regarding leakage power is high, though, it is important to highlight that the bigger the SRAM is, smaller becomes the power consumption overhead, since the proposed approach introduces an OCCS for each column of the SRAM. Finally, the technique significantly lowers the time necessary to identify problems within the SRAM's hardware and is able to detect defects that do not sensitize and are not detected by March testing techniques, but might cause faulty behaviour during the memory's lifetime. Nevertheless, the authors believe that the technique's ability to perform highly accurate detection without the need of a precedent threshold definition, using only information gained on-line, is to be considered the main contribution.

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