Analysis of Single-Event Upsets in a Microsemi ProAsic3E FPGA

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***Abstract* — The desirable use of Field-Programmable Gate Arrays (FPGAs) in aerospace & defense field has become a general consensus among IC and embedded system designers. Radiation-hardened (rad-hard) electronics used in this domain is regulated under severe and complex political and commercial treaties. In order to refrain from these undesired political and commercial barriers COTS FPGAs (despite the fact of their low reliability) have been considered as a promising alternative to replace rad-hard ICs. Moreover, SRAM-based FPGAs are pretermitted with respect to flash or anti-fuse devices. In this scenario, this paper analyses, by means of heavy-ion accelerator experiments, the Single-Event Upset (SEU) tolerance of the Microsemi ProAsic3E A3PE1500 COTS FPGA. This component is under pre-qualification process for use in some satellites of the Brazilian Space Program. Preliminary results are herein briefly presented and discussed. These experimental results allow us to consider this component as a strong candidate to replace rad-hard FPGAs, if its use is combined with strict system-level fault-tolerant strategies for error detection and correction.**

***Index Terms*— FPGA, SEU Sensitivity, Microsemi ProAsic3E, COTS, SEU pre-qualification.**

I. Introduction

Although the use of FPGA has become recurrent in commercial applications, its usage is avoided in space applications. As the space environment is much more aggressive than the ground-based one in terms of cosmic radiation and system recovering from failure is much more difficult (if not impossible), the use of *Field Programmable Gate Array*s (FPGAs) for such purpose faces severe criticism from the scientific community. Nonetheless, we observe an increasingly adoption of FPGAs in a large number of missions [1-4], since they fill several requirements for these projects, but always taking into account the fault tolerance due to the great influence of radiation and its effects in integrated circuits [5,6].

However, the vast majority of FPGAs used in space missions are *radiation hardened* (rad-hard) and not *Commercial off-the shelf* (COTS) devices. For some space programmes, one of the main motivations to use FPGAs is the possibility to implement fault-tolerant systems with COTS components. Depending on the country - such as in Brazil, the acquisition process of rad-hard components is controlled by government agencies, which imposes complex political and commercial barriers to access such technology.

On the other hand, given the Brazil's *National Institute for Space Research* (INPE) interest in upgrading the microprocessors used in the on-board computer (OBC) of their multi-mission platform, the soft-core LEON3 processor (SPARC V8) embedded on a COTS FPGA rises as a promising option. INPE's OBC employs the ERC32 microprocessor, which is a discontinued radiation-tolerant SPARC V7 architecture developed for space applications [7], and the adoption of a compatible SPARC architecture (e.g. LEON3) will avoid to redesign the whole source code from scratch, making easy also the porting of their RTEMS operating system.

In this scenario, the final goal of this paper is to analyze, by means of heavy-ion accelerator experiment, the Single-Event Upset (SEU) tolerance of the Microsemi FPGA ProAsic3E A3PE1500 COTS component. This device is cost-optimized: reprogrammable and nonvolatile. It is based on flash technology to store configuration bits, whereas volatile memory (in the form of FFs and SRAM cells) is used to store user data [9]. Some other ProAsic3E A3PE1500 device important characteristics for safe, critical applications are: (a) it supports 128-bit AES decryption for device configuration, (b) it is single chip and live at power-up and (c) 1,024 bits of user flash memory.

II. Methodology Description

The previous mentioned FPGA was configured with a logic written in *VHSIC Hardware Description Language* (VHDL) that mapped Flip-flop (FF) macros as an array. The Static RAM cells array of the FPGA was also mapped with specific pattern of 0's and 1's. Each FF and SRAM position represents an 18-bit wide structure. The entire process was run using the FlashPro software to read/write the FF and SRAM arrays via JTAG interface.

Two hardware configurations were submitted to radiation:

- The first configuration partially mapped the FFs and SRAM cells as an array of 18-bit 1,024 positions. The first half (512 positions) was fulfilled by FFs, whereas the second half addressed the SRAM cells. Each half comprised of a total of 9,216 bits.

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- The second configuration mapped the total storage capacity of the Microsemi ProAsic3E model A3PE1500 FPGA. In this case, we addressed 18,432 FFs and 276,480 SRAM bits, comprising the totality of 1,024 positions for FFs and 15,360 positions for the SRAM bits, both with 18-bit data wide.

A small set of 30 FFs was also used to ensure read/write control (via JTAG) of the FFs and SRAM cells depicted in the above two configurations. Table I summarizes the ProASIC3E resource usage for both configurations and the maximum resources available for the device. The reason for having two configurations is the *down-time* required by the JTAG logic to readback the whole set of configured memory elements (FFs and SRAM cells) outwards the FPGA. For configuration 2, this down-time is roughly 100 times larger than for configuration 1, which implied that the whole test time to run configuration 2 should be unaffordable long. This could cripple the entire test procedure.

Notice that FFs are sitting in the Core Logic (named VersaTiles by Microsemi). For the second configuration, we occupied 18,432 FFs, which represented 48.63% of the total number of FFs available in the FPGA. These 18,432 FFs were spread around 98.71% of the VersaTiles and were directly accessed from the host test computer via JTAG (i.e., they were not connected in a FIFO structure). It is worth noting that having targeted this direct-access read/write strategy for the FFs, we could not occupy 100% of the VersaTiles and more than 48.63% of the available FFs because of mapping restrictions in the RTL design-flow of the commercial Microsemi Libero Tool.

Table I. PROASIC3E Resources.

	Core Logic (VersaTiles)	FFs	SRAM Cells
Configuration 1	18624	9216	9216
Configuration 2	37903	18432	276480
Max. available	38400	n.a.	276480

Finally, for each test configuration, there were two possible initialization values, meaning the both configurations could be initialized with all positions set to logical "0" or "1". The goal of this procedure was to analyze if the probability of bit-flips from "0" to "1" is roughly equal to from "1" to "0".

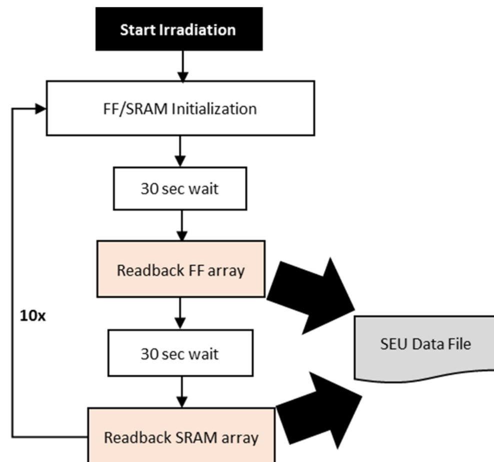
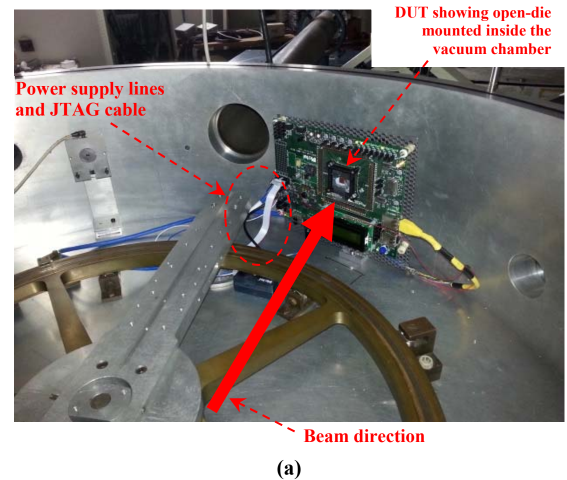


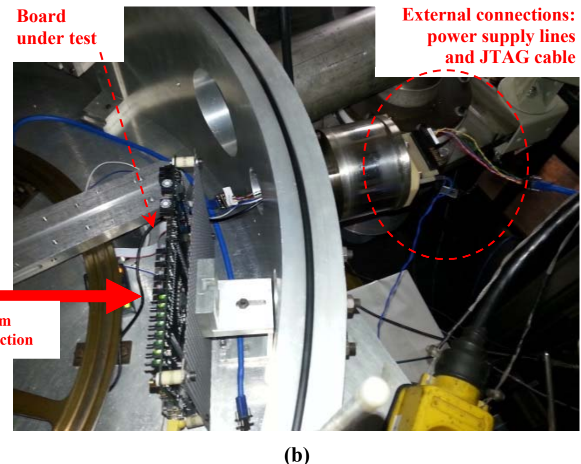
Fig. 1. Test Steps.

The test procedure is depicted in Fig. 1. Each round is initialized by configuring with "0" (resp. "1") the FF and SRAM cell arrays of the FPGA. Once configured the device, irradiation starts and after 30 seconds the FF array is readback. After another 30 seconds, the SRAM array is readback as well. This procedure is repeated 10 times and the readback data are stored in a text file for further analysis.

The SEU test was performed by exposing the ProASIC3E FPGA to heavy ions in an 8MV Pelletron [8] accelerator (Fig. 2 depicts the basics of the test setup). The device was irradiated with the following heavy ions: ^{12}C, ^{16}O, ^{19}F, ^{28}Si and ^{35}Cl.



(a)



(b)

Fig. 2. Test setup showing: **(a)** inside the vacuum chamber, the device under test and the test board; **(b)** the external connections: power supply lines and JTAG cable.

III. Obtained Results and Discussions

The configuration flash memory cells proved to be extremely robust to the set of irradiated particles, since no bit-flip was observed in these structures.

The cross section curve as function of LET for the SRAM cells of the FPGA ProAsic3E is shown in Fig. 3. As depicted in this figure for the ^{35}Cl element, bit-flips are observed in SRAM cells with a cross section on the order of $9.41 \times 10^{-9} cm^2/bit$. For the sake of comparison, in tests with Xilinx Spartan3E500 [10] bit-flips in SRAM cells (BlockRAMs) were observed with a cross section on the order of 4.14×10^{-9} cm^2/bit. In summary, Spartan3E BRAMs have demonstrated approximately half the

sensitivity to SEU than the ProAsic3E SRAM cells for elements with higher LET (^{28}Si and ^{35}Cl), while for lower LET elements (^{12}C and ^{16}O) this difference is less obvious (e.g. for the ^{12}C element: the SRAM ProAsic3E cross section is 4.0×10^{-9} cm^2/device whereas for the Spartan3E500 it is 2.56×10^{-9} cm^2/device). Nevertheless, the perception that the ProAsic3E SEU immunity is higher than the one of the Spartan3E for all four elements irradiated still persists.

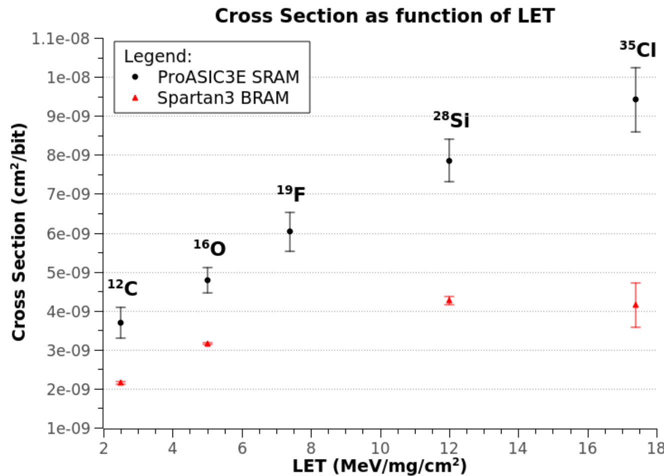


Fig. 3. "Cross section versus LET" for the SRAM cell array of the ProAsic3E FPGA (comparison with experimental data extracted from Xilinx Spartan3E500 [10]).

Fig. 4 presents the cross section versus LET for the SRAM cells array obtained by computing the number of bit-flips from "0" to "1" (SRAM – 0) and "1" to "0" (SRAM – 1). As observed, for low-LET elements (^{12}C and ^{16}O) there is a slight tendency of a higher SEU cross section for bit flips from "0" to "1" than from "1" to "0". However, this tendency is not observed for high-LET elements (^{28}Si and ^{35}Cl). We suppose that this slight tendency can be explained due to layout differences in the sensitive volumes of the nMOS and pMOS transistors, where the considered information is stored. If true, this hypothesis could confirm the slight difference of SEU sensitivity for storing 0's and 1's. Note that to provide a more confident answer, it would be necessary to know details about the device layout.

Fig. 5 presents the cross section versus LET for the FFs array obtained by computing the number of bit-flips from "0" to "1" (FF – 0) and "1" to "0" (FF – 1). However, contrary to the results observed for the SRAM cells array (Fig. 4), we cannot observe difference on the SEU cross section as a function of LET for bit flips from "0" to "1" and from "1" to "0".

Finally, Fig. 6 compares the SEU cross section as function of LET between the arrays of SRAM cells and FFs. As observed, FFs are roughly twice more sensitive to SEUs than SRAM cells for high-LET elements (^{28}Si and ^{35}Cl). However, this tendency is not observed as long as we move towards low-LET elements such as ^{12}C and ^{16}O, which present similar sensitivity to SEU.

As the explanations for bit flips observed from "0" to "1" and from "1" to "0" seen in Fig. 4, hereafter we also assume that the higher SEU sensitivity observed for FFs in comparison to SRAM cells can be explained because of layout differences in the sensitive volumes of the nMOS and pMOS transistors. If true, this hypothesis could confirm the slight difference of SEU sensitivity observed by FFs in comparison to SRAM cells.

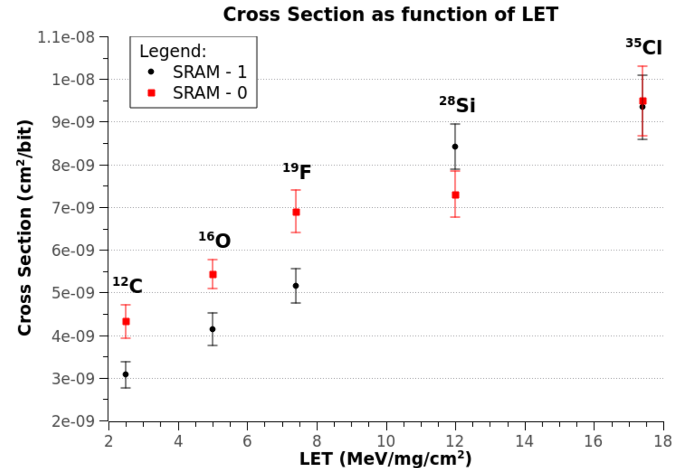


Fig. 4. "Cross section versus LET" for the SRAM cell array of the ProAsic3E FPGA (comparison between bit-flips from "0" to "1" and "1" to "0").

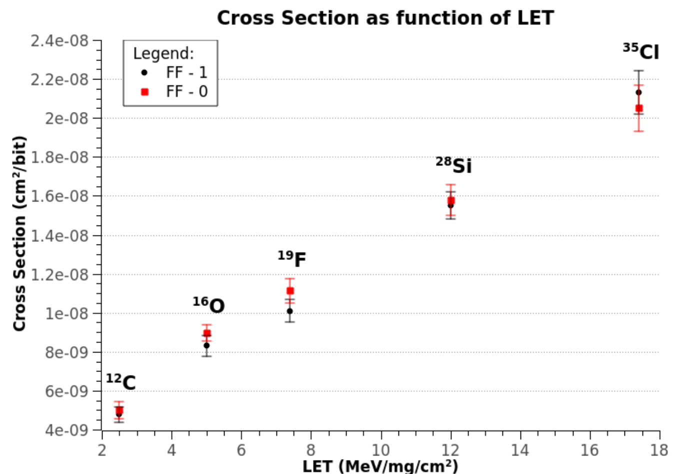


Fig. 5. "Cross section versus LET" for the FF array of the ProAsic3E FPGA (comparison between bit-flips from "0" to "1" and "1" to "0").

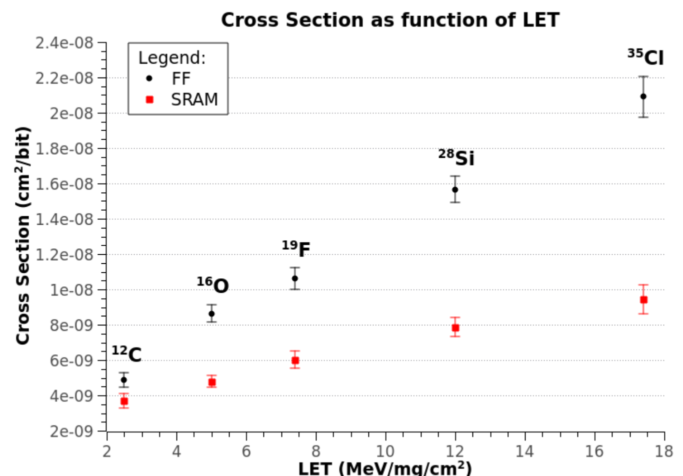


Fig. 6. Cross section comparison between the arrays of SRAM cells and FFs (depicted values are the average bit-flips from "0" to "1" and "1" to "0").

IV. Final Discussions and Conclusions

As stated before, the Brazil's *National Institute for Space Research* (INPE) is interested in replacing the ERC32 legacy processors used on their on-board computers by a compatible LEON3 soft-core processor embedded in a COTS flash-based FPGA. This design decision has been made considering the difficulties faced to import radiation-hardened devices, and also to avoid unnecessary work in the porting process of the on-board computer's existing source code and operating system

In this scenario, this paper presented a preliminary analysis about the Single-Event Upset (SEU) tolerance of the Microsemi ProAsic3E A3PE1500 COTS FPGA under heavy-ion accelerator experiment. This component is under pre-qualification process for use in some satellites of the Brazilian Space Program. Experimental results were briefly presented and discussed. These results allowed us to consider this component as a strong candidate to be included in the Brazilian Space Program, if its use is combined with strict system-level fault-tolerant strategies for error detection and correction.

Among the obtained results, we observed that:

(1) Spartan3E BRAM cells have demonstrated approximately half the sensitivity to SEU than the ProAsic3E SRAM cells for all four elements irradiated.

(2) FFs present in the core logic (VersaTiles) of the ProAsic3E FPGA are more sensitive to SEU than the SRAM cells. This sensitivity hangs from around 20% more sensitive (for low-LET elements such as ^{12}C and ^{16}O) to slightly more than 100% (for high-LET elements: ^{28}Si and ^{35}Cl).

(3) The cross-section for the SRAM cells array of the ProAsic3E was measured for bit-flips from "0" to "1" and from "1" to "0". As observed, for low-LET there is a slight tendency of a higher SEU cross section for bit flips from "0" to "1" than from "1" to "0". For high-LET, the measured cross section has shown to be similar in both directions, i.e., from"0" to "1" and vice-versa. Moreover, we measured the FFs cross section. In this case, the observed cross section has shown to be similar in both directions, for all irradiated elements.

In an on-going work, a more complete set of SEU experiments is under development in order to confirm the above preliminary results. Additionally, we expect to perform a combined total-ionizing dose (TID) and SEU test of this component to understand the SEU sensitivity as a function of different TID levels deposited on the FPGA. This type of test, though more complex, is fundamental if we want to understand the influence of total-ionizing dose (TID) radiation on the SEU sensitivity.

Acknowledgements

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References

[1] C. A. Kletzing, W. S. Kurth, M. Acuna, R. J. MacDowall, R. B. Torbert, T. Averkamp, D. Bodet, S. R. Bounds, M. Chutter, J. Connerney, D. Crawford, J. S. Dolan, R. Dvorsky, G. B. Hospodarsky, J. Howard, V. Jordanova, R. A. Johnson, D. L. Kirchner, B. Mokrzycki, G. Needell, J. Odom, D. Mark, R. Pfaff, J. R. Phillips, C. W. Piker, S. L. Remington, D. Rowland, O. Santolik, R. Schnurr, D. Sheppard, C. W. Smith, R. M. Thorne, and J. Tyler. "The electric and magnetic field instrument suite and integrated science (emfisis) on rbsp". *Space Science Reviews*, 179(14):127–181, 6 2013.

[2] Robert Glein. "Bram radiation sensor for a self-adaptative seu mitigation". *SpacE FPGA Users Workshop*, 2014.

[3] Malcolm S. Mollison, Jeremy P. Erickson, James H. Anderson, Sanjoy K. Baruah, and John A. Scoredos. "Mixed-criticality real-time scheduling for multicore systems". *2010 10th IEEE International Conference on Computer and Information Technology*, pp. 1864–1871. IEEE, 6 2010.

[4] Nan Guan and Wang Yi. "Fixed-priority multiprocessor scheduling: Critical instant, response time and utilization bound". *2012 IEEE 26th International Parallel and Distributed Processing Symposium Workshops & PhD Forum*, pp. 2470–2473. IEEE, 5 2012.

[5] Cinzia Bernardeschi, Luca Cassano, and Andrea Domenici. "SRAM-based FPGA systems for safety-critical applications: A survey on design standards and proposed methodologies". *Journal of Computer Science and Technology*, 30(2): 373–390, 3 2015.

[6] D. Sabena, L. Sterpone, Mario Scholzel, Tobias Koal, H. T. Vierhaus, S. Wong, R. Glein, F. Rittner, C. Stender, M. Porrmann, and J. Hagemeyer. "Reconfigurable high performance architectures: How much are they ready for safety-critical applications?" *2014 19th IEEE European Test Symposium (ETS)*, pp. 1–8. IEEE, 5 2014.

[7] European Space Agency (2016). ERC32 page at ESTEC. [Online]. Available: http://microelectronics.esa.int/erc32/erc32.html

[8] V.A.P. Aguiar, N. Added, N.H. Medina, E.L.A. Macchione, M.H. Tabacniks, F.R. Aguirre, M.A.G. Silveira, R.B.B. Santos, and L.E. Seixas. "Experimental setup for single event effects at the sao paulo 8ud pelletron˜ accelerator". *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms*, 332: 397–400, 8 2014.

[9] Microsemi Corporation (2016). ProASIC3e FPGAs. [Online]. Available: www.microsemi.com/products/fpga-soc/fpga/proasic3-e

[10] Juliano Benfica, Bruno Green, Bruno C. Porcher, Leticia Bolzani Poehls, Fabian Vargas, Nilberto H. Medina, Nemitala Added, Vitor A. P. de Aguiar, Eduardo L. A. Macchione, Fernando Aguirre, Marcilei A. G. da Silveira, and Eduardo A. Bezerra. "Analysis of SRAM-based FPGA SEU Sensitivity to Combined Effects of Conducted EMI and TID. *2015 15th European Conference on Radiation and Its Effects on Components and Systems (RADECS)*, pp. 1–4. IEEE, 9 2015.