2016 29th International Conference on VLSI Design and 2016 15th International Conference on Embedded Systems

Analyzing the Impact of SEUs on SRAMs with Resistive-Bridge Defects

G. Cardoso Medeiros, L. Bolzani Poehls, F. Vargas
School of Engineering
Pontifical Catholic University of Rio Grande do Sul - PUCRS
Porto Alegre, Brazil
leticia@poehls.com

***Abstract*—The constant evolution and miniaturization of nanotechnology brought many revolutions to semiconductors, making the improvement of the Integrated Circuit manufacturing process necessary. Alongside, the increasing need to store more and more information as well as the device's high density, have resulted in the fact that Static Random Access Memories (SRAMs) occupy great part of Systems-on-Chip (SoCs). However, such evolution has led to the occurrence of manufacturing defects that may affect IC reliability and cause yield loss. Moreover, technology scaling has also brought attention to soft errors, which can be caused by inherent environmental noise. When considering both aspects, memory cells affected by weak resistive manufacturing defects, although not impaired under typical environments, may present peculiar behaviors when exposed to factors that can cause Single-Event Upsets (SEUs). In this context, this paper proposes to analyze the impact of environmental noise, in particular EMI and radiation, in SRAM cells with weak resistive-bridge defects that may escape manufacturing test due to their dynamic behavior. The proposed combined analysis has been performed using SPICE simulations adopting a commercial 65nm CMOS technology library.**

Keywords—SRAMs; Resistive-Bridge Defects; EMI; Radiation; SEUs

I. INTRODUCTION

Advances in nanometer technology have made the integration of hundred million transistors into a small area, not larger than a few square centimeters, possible; allowing the increase of circuits' density. In parallel, the always increasing need to store more and more information has resulted in the fact that Static Random Access Memories (SRAMs) occupy great part of the Systems-on-Chip's (SoCs') silicon area. In other words, memory has become the main contributor to the overall SoC area. The SIA Roadmap forecasted a memory density approaching 94% of the SoC's silicon area for 2015 [1].

On the one hand, the most critical downside of technology scaling beyond the 65nm node is related to the non-determinism of the devices' electrical parameters due to process variation [7][8]. This type of variation is mostly caused by random fluctuations of dopant atoms and can be observed as a fixed deviation from the device's nominal behavior [9]. Thus, technology scaling has led to the development of new types of manufacturing defects that may assume a dynamic behavior. A resistive-bridge defect creates a connection between two nodes that should have no relation and is caused by inconsistencies and imperfections in the manufacturing process [11]. In more detail, the new connection has a fixed resistance value that depends on its shape and the materials involved. Note that if the resistance of the new connection is sufficiently small, the circuit will be affected by a delay large enough to cause failures, which can be detected by traditional test methods. Nevertheless, if the resistance is not significantly small, the defect will not necessarily be able to cause a faulty behavior, which impacts on SRAM reliability. These weak defects generally cause timing dependent faults, which means that at least a 2-pattern sequence is necessary to sensitize them [5]. According to [4], faults requiring a large number of at-speed operations on each memory cell for sensitization are denominated dynamic faults.

On the other hand, inherent environmental noise may affect IC's behavior causing Single Event Effects (SEEs). Technology scaling has been exacerbated the susceptibility of ICs to environment, since the physical size of cells has been reduced implying on a scale-down in the junction area and a reduction in capacitance, leakage as well as operating voltage. In every generation, operating voltage and node capacitance decrease at a rate of 30%, representing an exponential drop in the charge used to represent a logic value [12]. Therefore, a small interference may already change the state of the cell. Thus, when environment noise, Electromagnetic Interference (EMI) or radiation, affects a memory cell, it can cause a Single Event Upset (SEUs) in the affected cell as well in neighboring cells. These bit-flips are produced by single charged particles that strike the transistor's drain. Particles lose energy by hitting the ICs and produce electron hole pairs, creating a dense ionized track in the local region. Consequently, the ionization causes a transient current pulse, which can produce a SEU, thus flipping the value stored in the cell. Until a new value is written, the wrong data remains stored.

In this context, this paper proposes to analyze the impact of SEUs on SRAM cells that have been affected by some kind of nominal behavior deviation caused by process variation associated to the manufacturing process. In more detail, the main idea behind this paper is to provide an evaluation of SEU's impact on SRAM cells that are affected by weak resistive-bridge defects that may escape test procedures due to their dynamic behavior. Note that the usually adopted test

978-1-4673-8700-2/16 $31.00 © 2016 IEEE
DOI 10.1109/VLSID.2016.146

procedures, mostly designed in order to detect static faults, are not able to detect dynamic faults. In fact, the detection of dynamic faults poses significant challenges related to the necessity of performing at-speed testing as well as a large number of operations on each memory cell, depending on the defect size present in the SRAM cell. Basically, the defect size defines if a fault is classified as static or dynamic. Thus, some particular defects that may have not been detected during manufacturing test, may cause dynamic faults during the SRAM's operation in the field, when exposed to environment noise. Experimental results obtained through SPICE simulations using a commercial 65nm CMOS technology library represent a first analysis evaluating the reliability of SRAM cells affected by weak resistive-bridge defects when exposed to harsh environments.

The paper has been organized as follows: in Section II the background related to SRAM as well as environment noise SEUs are laid out and the assumed resistive-bridge fault model for SPICE simulations is described. Section III describes the experimental setup adopted, whereas Section IV discusses the obtained results. Finally, Section V presents the final considerations of this work.

II. BACKGROUND

As previously mentioned, process variation has led to the introduction of new manufacturing defects that may generate dynamic faulty behaviors during the operation of defective cells. Indeed, SEUs have emerged as one of the most important sources of transient faults on memory cell due to the technology miniaturization. Thus, in this Section, the main characteristics of the SRAM cell, radiation and EMI effects on defective cells and the fault model adopted to represent resistive-bridge defects in SRAM cells will be summarized.

A. The SRAM Cell

A standard six-transistor SRAM cell, composed of four transistors that form two cross-coupled CMOS inverters and two nMOS transistors that provide read and write access to the cell, is adopted in this work. The transistor sizing has been determined to be a reasonable trade-off between cell density and robustness. This choice results in the following transistor sizing values: (a) The ratio between pull-down and access transistors (Rd), where Rd = Wpull-down/Waccess = 0.18nm/0.12nm = 1.5; and (b) the ratio between pull-up and access transistors (Rp), where Rp = Wpull-up/Waccess = 0.20nm/0.12nm = 1.67. Note that these values assure the SRAM cells' stability against a noise of 200mV during read operations. Finally, the basic SRAM cell has been mapped into a commercial 65nm CMOS technology library.

B. Fault Model Associated to Resistive-Bridge Defects

During the manufacturing process, a standard six-transistor SRAM cell can be produced including resistive-bridge defects that may modify the correct behavior of the memory cell. These defects can be functionally characterized according to the fault model presented in [13]. In more detail, this fault model represents the set of the following faulty behaviors:

- *Stuck-at Fault* (SAF): A cell is said to have an SAF when it is unable to store both logic values. *Stuck-at 1* represents a cell that cannot store logical value '0', while *Stuck-at 0* represents the opposite.
- *Read Destructive Fault* (RDF): A cell is said to have an RDF if a read operation performed on the cell changes the data in the cell and returns an incorrect value on the output. Note that this type of fault can also have a dynamic behavior, being classified as dRDF;
- *Deceptive Read Destructive Fault* (DRDF): A cell is said to have a DRDF if a read operation performed on the cell returns the correct logic value, and it changes the contents of the cell. This type of fault can also have a dynamic behavior classified as dDRDF;
- *Incorrect Read Fault* (IRF): A cell is said to have an IRF if a read operation performed on the cell returns an incorrect logic value, and the correct value is still stored in the cell;
- *Weak Read Fault* (WRF): A cell is said to have a WRF when the ΔV between inverters is not enough for the sense amplifier to produce the correct logic output.

As previously mentioned, a fault classified as dynamic is caused by a resistive defect that demands a write operation followed by multiple read operations in sequence in order to sensitize the faulty behavior [13]. The number of read operations depends on the defect size. Fig. 2 depicts the scheme adopted to model the previously described faults.

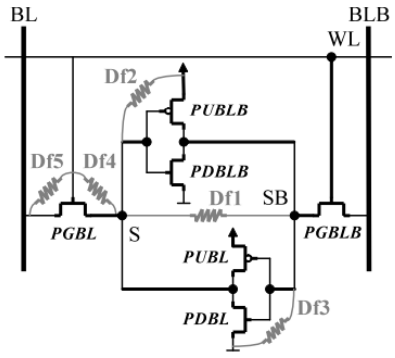

Fig. 1. Resisitive-bridge defects injected into an SRAM cell [13].

The five resistive-bridging defects can be classified into two groups [13]:

- *Group_1:* This group includes defects that may affect the behavior of the core-cell when read and/or write operations are performed on it. Defects associated to Group_1 involve single-cell faulty behaviors and include Df1, Df2 and Df3. Thus, these defects may impact electric nodes within the core-cell only;
- *Group_2:* This group includes defects affecting the behavior of the defective core-cell and of other non-defective core-cells of the array. Defects associated to Group_2 may involve double-cell faulty behaviors. Group_2 includes Df4 and Df5, as these defects may impact BL and WL nodes.

According to [13], SAFs can be modeled using Df2, Df3 or Df4. RDF or dRDF can be observed injecting Df1, Df2, Df3, or Df5. There are no reports of DRDF or dDRDF with the injection of these defects. Finally, IRF can be caused by Df4 or Df5, while WRFs can be modeled using all defects described. It is important to highlight that the faulty behaviors associated to each defect reported in [13] differ from the ones identified in this paper. Due to the exhaustive simulations performed in this work, many faults related to each defect complemented the set of faults reported in [13].

C. *EMI and Radiation Effects*

EMI and radiation can affect the behavior of SRAM cells. Basically, inherent environment noise may cause SEUs in the affected cell as well in neighboring cells. Fig. 1 depicts particles striking the drain of a transistor.

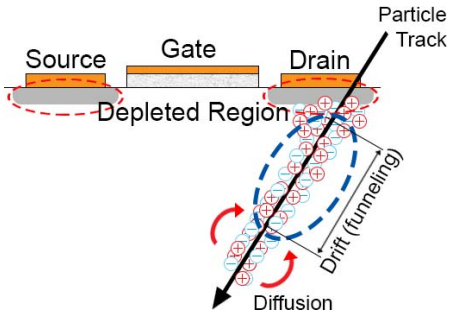

Fig. 2. Partricles striking a transistor.

III. EXPERIMENTAL SETUP

In order to provide the proposed analysis, electrical simulations have been performed adopting an SRAM, composed of 1024 lines of 8 columns each connected to the functional blocks, using a 65nm technological library by STMicroelectronics considering the corner defined as typical, with the temperature set to 27ºC and the voltage to 1.0V. Thus, the impact of SEUs on SRAM cells with weak resistive-bridge defects has been evaluated performing simulations. The comparison of these results serves to understand if certain weak defects, which may escape manufacturing test, reduce the reliability of SRAM cells by causing faulty behaviors when exposed to harsh environments. Note that more extensive simulations would have to be performed in order to allow a more exact relation between defect size and the cell's power consumption when under the influence of radiation and EMI.

It is also important to emphasize how relative the analysis of SEUs on memory cells may be. To fully understand its impact, it is necessary to evaluate all possible cases of impact. Thus, to determine the critical charge – which is the required current to cause a bit-flip on a memory cell, it is necessary to consider not only the magnitude of the current pulse, but also other parameters, such as the value the cell stores, the direction of the pulse, and state of operation of the affected cell. Some setups can be ignored as there would be no effect, e.g. removing charge from a node that is storing '0'.

In a first step, SEU's impact has been evaluated considering a defect-free SRAM. Fig. 3 depicts the critical charge, in *Amperes*, to cause a bit-flip on an SRAM cell storing '0' when it is performing no operation – in other words, in a static mode. Observing Fig. 3 it is possible to see that, considering the adopted experimental setup, two different models required two different critical charges. In the first setup, the current pulse is removing charge from the cell, and 136µA is already sufficient to cause a bit-flip. However, on the second setup, the current pulse is depositing charge on the cell and in this case, greater pulse to observe a bit-flip was necessary.

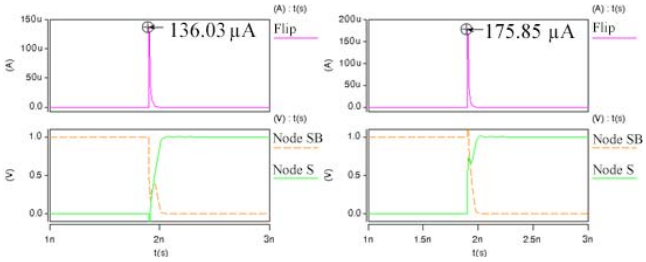

Fig. 3. Stored value (V) of the defect-free SRAM cell over time being affected by current pulses (A), causing SEUs on the cells.

When there is no defect in a cell, the cell is completely symmetric. Thus, it is reasonable to assume that the charge necessary to cause a bit-flip by removing charge from a cell that is storing '0' is exactly the same necessary to cause a bit-flip by removing charge on a cell that is storing '1'.

Regarding dynamic modes, both read and write operations have two distinct moments: when the word line is active and the cells have direct access to the bit lines, and when the word line is off, thus leaving a cell in a static state – even though an operation is being performed on the cell. Therefore, in those moments when the cell does not have contact to the bit lines, the critical charge necessary to cause a bit flip is the same observed when the cell is not being stressed.

During the first stage of the read operation, the cell has direct access to the bit lines. The cell suffers from stress, which causes a drop on S' voltage and an increase in SB's voltage if the cell is storing '1' (the opposite happens if the cell is storing '0'). Thus, the critical charge for this case is smaller than the critical charge in a static mode. In addition, the same symmetrical behavior was observed during the first stage of a read operation. Thus, the observed critical charge during the first stage of a read operation on a cell storing '0' is the same critical charge observed during the first stage of a read operation on a cell storing '1'. As for write operations, a defect-free cell is not affected by SEUs during its second stage, when the cell has direct access to the bit lines. This is due to the fact that bit lines are not equally charged, which causes the cell to lean to the value that is being written, despite the current pulse.

In a second step, the relation between defect size and faulty behavior has been identified in order to understand how to simulate weak resistive-bridge defects. As stated previously, resistive-bridge defects are connections between two nodes that should have no relation. Because of their nature, these defects may cause functional faults from low resistances up to a defined threshold. Thus, to determine the resistance threshold and the faults caused by these defects, it is

inserted a small-resistance defect in the cell. This defect's resistance is then enhanced, until no fault is observed.

Table I summarizes the simulations performed in order to establish the threshold between a faulty and a fault-free behavior based on the injected defects' size for each injection position, see Fig. 2. It is possible then to identify when the defect's size is small enough to characterize a static or dynamic fault in SRAM c2ell, or when the defect inserted in the SRAM cell is great enough and consequently does not sensitize a faulty behavior, characterizing a weak-resistive defect.

TABLE I. RELATION BETWEEN DEFECT SIZE AND FAULTY BEHAVIOUR.

Df*i*	Observed Fault	Maximum Resistance [kOhm]
Df1	NSF	36.5
	RDF	39.5
	dRDF	41.5
	IRF	44.5
	dWRF	47.5
Df2	SA1	11.5
	RDF	13.0
	TF1→0	22.5
Df3	SA1	18.5
	TF1→0	22.5
	RDF	70.0
	DRDF	74.0
Df4	IRF	12.0
	SA0	18.0
	TF0→1	18.0
	TF1→0	21.5
Df5	dRDF	0.25
	TF1→0	1.60
	IRF	16.0
	WRF	18.0
	TF0→1	61.5
Df5 (Array)	RDF	15.0
	IRF + dRDF	25.0
	IRF	36.0
	dIRF	38.5
	TF0→1	60.0

Observing Table I, it is possible to see that resistive-bridge defects act from low resistances up to a maximum threshold; an evolution between faults is observed in most cases, which consists in the merge of two faults or the dynamic behavior of a fault that was already observed.

IV. RESULTS

This Section summarizes the main results obtained during the simulations performed in order to provide information for the analysis proposed in this paper. The next figures depict the SEU impact when considering SRAM cells in the presence of some of the resistive-bridge defects previously described.

Fig. 4 depicts the SRAM cell functional behavior, *Volts* over *nanoseconds*, in the presence of a Df1 equals to 50kOhm. This value has been selected considering that a Df1 equal or smaller than 47.5kOhm is able to sensitize faults at logic level. Thus, the value of 50kOhm is within the defect size range that may not be sensitized at logic level, which means that no faulty behavior can be observed during read and write operations. Observing Fig. 4 it is possible to see that a 100µA can cause a bit-flip on this defective cell, while such soft-error would not happen on a defect-free cell (as shown on the right).

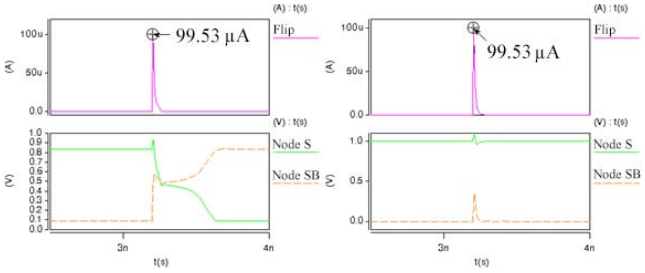

Fig. 4. Faulty behavior: stored value (V) related to Df1 and a defect-free cell when exposed to induced current pulses.

As this defect causes a significant drop in the ΔV between S and SB nodes during a read operation, it is necessary a very little amount of charge to cause a bit flip during the second stage of such operation. Fig. 5.a illustrates the case of a current pulse depositing charge during the second stage of a read operation (when the word line is off), while Fig. 5.b illustrates the case of a current pulse removing charge. For the exact same setup on a defect-free cell, it is necessary a current of 152.6µA and 175µA to cause a bit flip, respectively. In other words, a cell affected by a 50kOhm weak-resistive defect connecting S and SB nodes will be 90% more vulnerable to SEUs removing charge during the second stage of a read operation, and 92% more vulnerable to SEUs depositing charge in the same situation.

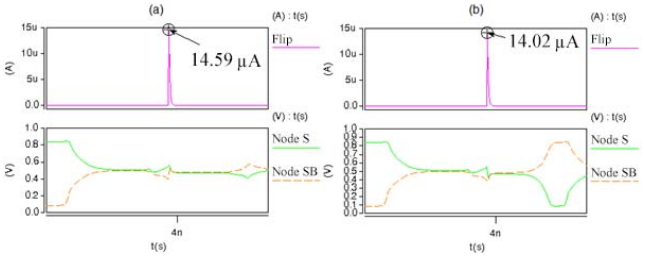

Fig. 5. Faulty behavior observed during dynamic mode related do Df1.

Most resistive-bridge defects have a negative impact on cell's reliability when exposed to radiation and EMI. Fig. 6 depicts an SRAM cell affected by a 75kOhm Df3; such defect magnitude is considered a weak-resistive defect and does not trigger any fault, thus this cell would be considered functional after manufacturing tests. This defect makes the cell extremely vulnerable to SEUs during the read operation; if a current pulse strikes the cell meanwhile a read operation is being performed, it is most likely that this cell will suffer a bit flip. While it is necessary to deposit 152µA on S to observe a bit-flip on a defect-free cell, a 14.6µA current pulse already causes a bit-flip on a cell affected by a 75kΩ defect. This represents 90.5% less charge to cause a SEU. This critical charge is even smaller when removing charge from SB: it is possible to observe bit flips on the cell when removing charges as little as 5µA, which

represents a critical charge 93% smaller than the one required to cause a bit flip on a defect-free cell.

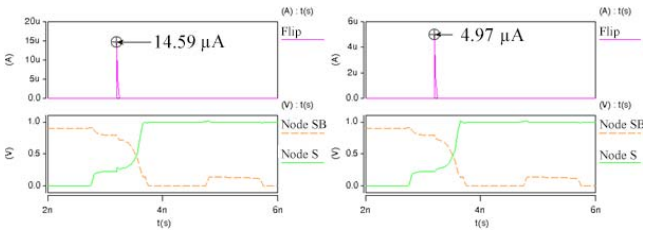

Fig. 6. Faulty behavior observed during dynamic mode related do Df3.

Fig. 7 depicts an SRAM cell affected by a 23kOhm Df2. After several tests, this cell would be marked as defect-free and perfectly functional, as no fault would be observed. Yet, once exposed to external noise, this cell would show peculiar behaviors based on the state of the cell and the characteristics of the current pulse. If the cell is storing the logic value '0', it is necessary to deposit 116µA on S to observe a bit-flip. This critical charge represents almost 34% less charge to cause a bit flip, comparing to a defect-free cell on the same setup.

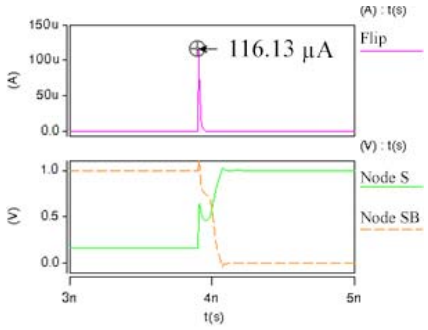

Fig. 7. Faulty behavior: store value (V) related to Df2 during static mode.

However, in some setups, the presence of this defect turned the cell more robust against the effects of single-event upsets caused by transient current pulses. As this defect hinders the voltage decrease on node S, it is necessary to remove a greater amount of charge from S to cause a bit-flip is greater than the charge necessary to cause a bit-flip on the same setup considering a defect-free cell. Thus, this defect makes the defect cell more robust against current SEUs that remove charge from S. If the cell is storing '1', it is necessary to remove 50% more charge to cause a bit flip on the defective cell, as illustrated in Fig. 8.

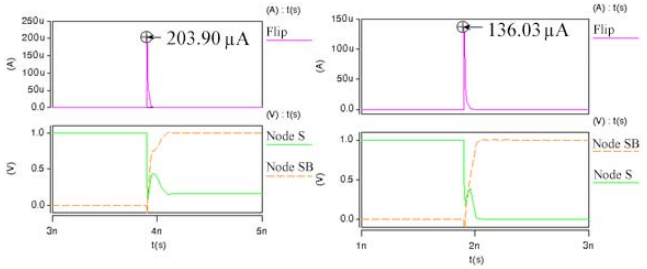

Fig. 8. Comparison between critical charges observed on a cell afected by a Df2 and a defect-free cell.

This increase in robustness is also observed in other setups in cells affected with other resistive-bridge defects. Fig. 9 depicts the SRAM cell functional behavior, *Volts* over *nanoseconds*, on a dynamic mode operation and in the presence of a Df4 equals to 23kOhm, which would not cause any fault during manufacturing tests; such defect is thus considered a weak-resistive defect. During the first stage of a read operation, the cell becomes more robust when the logic value '1' is stored and the induced current pulse is removing charge from S. As the word line is active throughout the first stage of this operation, this signal supplies voltage to node S, thus requiring a greater amount of charge to be removed to cause a bit flip; it is necessary 40% more charge to cause a bit flip, considering that the critical charge for this setup on a defect-free cell is 73µA.

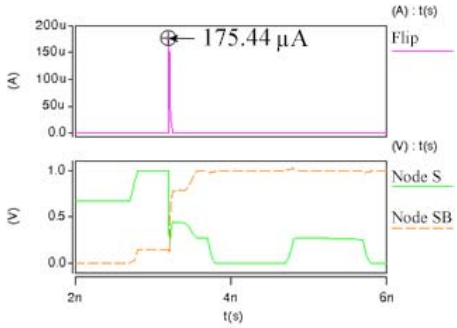

Fig. 9. Faulty behavior: output value (V) related to Df4 on a dynamic mode while storing the logic value '1'.

Nevertheless, this increase in robustness does not aggregate any improvement when considering the trade-off in vulnerability. All defects that turned memory cells more robust in some setups also made them more vulnerable in other setups. Fig. 10 depicts the same SRAM cell illustrated in Fig. 9, but this time the cell stores the logic value '0'. As the word line signal will be supplying voltage to S due to the connection created by Df4, it takes less charge to cause the stored value to flip, making the cell more vulnerable during the read operation. It is necessary to deposit 94µA on S to observe a bit flip, which represents almost 40% less charge if compared to a defect-free cell; as for removing charge from SB, the critical charge observed is 25µA, which represents 65% less charge.

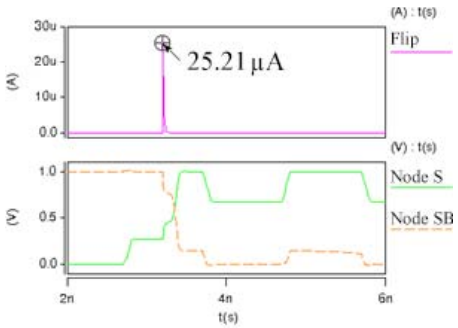

Fig. 10. Faulty behavior: output value (V) related to Df4 on a dynamic mode while storing the logic value '0'.

In the set of possible defects simulated in this work, Df5 is the only one capable of affect other cells beyond the one with the defect, as the defect is located in the bit line. Thus, if a cell (the *aggressor*) is affected by this defect, all other cells in the same column (the *victims*) may (and most likely will) suffer as well. When evaluating the impact of SEUs on cells affected by this defect, it is observed no difference between critical charges in a defect-free cell and a defective cell; the charge necessary to cause a bit flip is the same as if the defect did not exist. This behavior was observed in all setups, except for *w1* operations. In all other setups explored in this work, regardless if it was affected by a defect or not, it was not possible to cause a bit-flip during the second stage of the write operation (when the word line signal is on). This happens because one of the bit lines always forces their state on the cell, thus preventing a bit flip. Df5 makes the bit line weak, thus during the first stage of the read operation, the signal is not properly charged to hold to a SEU.

To finalize the analysis, Fig. 11 depicts the distribution of setups in which the critical charge observed was different from a defect-free cell. Of all 44 setups, 26 required less charge while 18 required more. This represents a 60%-40% relation. Furthermore, only two setups required 30% or less charge to cause a bit flip, of all 26 that turned the cell more vulnerable. For setups where the cell became more robust, seven of them required at maximum 30% more charge. This represents only 7% of all setups that turned the cell more vulnerable, and 38% of all setups that turned the cell more robust.

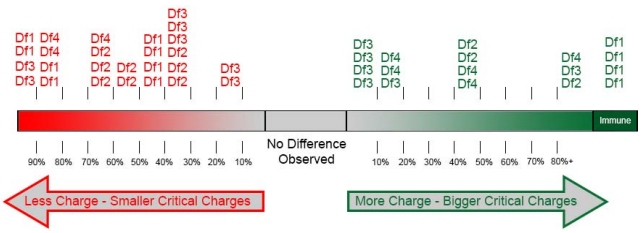

Fig. 11. Distribution of resistive-bridge setups that reported a different critical charge from a defect-free cell.

V. Final Considerations

This paper presents an analysis of the impact of induced current pulses caused by radiation and electromagnetic interference on SRAM cells with weak resistive-bridge defects that may escape manufacturing tests. The main reason for the proposed analysis is associated to the fact that certain weak resistive-bridge defects, which are not propagated to the logic level, may cause faulty behaviors on SRAM cells when exposed to harsh environments. In other words, defects that initially did not represent a reliability problem, because they are not able to sensitize any faulty behavior and were considered to be weak, may become a source of faults after the cell was affected by Single Event Upsets.

It became clear that resistive-bridge defects alter the stability of static random access memories. Most defects had both positive and negative effects on the cell, increasing the vulnerability to some operations while turning the cell more robust to others. However, it is also possible to say that the vulnerability emerged with the defect is much more significant than the robustness.

Acknowledgment

This work has been partially supported by CNPq (Science and Technology Foundation, Brazil) under contracts n. 301726/2008-6 and n. 556761/2009-0 and by FAPERGS/ CAPES 014/2012.

References

[1] Semiconductor Industry Association (SIA), “International Technology Roadmap for Semiconductors (ITRS)”, 2005 Edition.

[2] J. C.-M. Li, C-W Tseng, E. J. McCluskey, “Testing for Resistive Opens and Stuck Opens”, IEEE International Test Conference, 2001.

[3] W. Needham, C. Prunty, H. Z. Eng, “High Volume Microprocessor Test Escapes, an Analysis of Defets our Tests are Missing”, IEEE International Test Conference, 1998.

[4] P. Dubey, A. Garg, S. Mahajan, Study of Read Recovery Dynamic Faults in 6T SRAMs and Method to Improve Test Time, Journal Electron Test, 2010.

[5] S. Borri, M. Hage-Hassen, L. Dilillo, P. Girard, S. Pravossoudovitch, A. Virazel, “Analysis of Dynamic Faults in Embedded-SRAMs: Implications for Memory Test”, JETTA, 2003.

[6] K. Zhang, U. Bhattacharya, Z. Chen, F. Hamzaoglu, D. Murray, N. Vallepalli, Y. Wang, B. Zheng, M. Bohr, “SRAM Design on 65-nm CMOS Technology With Dynamic Sleep Transistor for Leakage Reduction”, IEEE Journal of Solid-State Circuits, Vol. 40, N. 4, April 2005.

[7] D. Boning, S. Nassif, “Models of Process Variations in Device and Interconnect”, Design of High Performance Microprocessor Circuits, IEEE Press, 2000.

[8] S. Borkar, “Designing Reliable Systems from Unreliable Components: The Challenges of Transistor Variability and Degradation”, IEEE Micro. 25, 6, 10–16, 2005.

[9] A. Alam, “Reliability- and Process-Variation Aware Design of Integrated Circuits”, Microelectronics Reliability, Vol. 48, Issues 8-9, pp. 1114–1122, Aug-Sept 2008.

[10] L. Dilillo, P. Girard, S. Pravossoudovitch, A. Virazel, “Analysis and Test of Resistive-Open Defects in SRAM Pre-Charge Circuits”, Journal of Electronic Test: Theory and Applications, 2005.

[11] A. Bosio, et al., “Advanced Test Methods for SRAMs”, Springer Science+Business Media, LLC 2010.

[12] H. V. Minaya, “Reliability Enhancement of Nanometer-Scale Digital Circuits”, Thesis (PhD in Electrical Engineering) - National Institute for Astrophysics, Optics and Electronics. Tonantzintla, Puebla, Mexico. May 2014.

[13] R. A. Fonseca, L. Dilillo, A. Bosio, P. Girard, S. Pravossoudovitch, A. Virazel, N. Badereddine, “Analysis of resistive-bridging defects in SRAM core-cells: A comparative study from 90nm down to 40nm technology nodes”, Test Symposium (ETS), 2010 15th IEEE European , vol., no., pp.132,137. 24-28 May 2010