Pontifical Catholic University of Rio Grande do Sul - PUCRS

School of Engineering

Graduate Program in Electrical Engineering

Guilherme Cardoso Medeiros

Development of a Test Methodology for FinFET-Based SRAMs

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Advisor: Leticia Maria Bolzani Poehls, Ph.D.

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DEVELOPMENT OF A TEST METHODOLOGY FOR FINFET-BASED SRAMS

CANDIDATO: GUILHERME CARDOSO MEDEIROS

Esta Dissertação de Mestrado foi julgada para obtenção do título de MESTRE EM ENGENHARIA ELÉTRICA e aprovada em sua forma final pelo Programa de Pós-Graduação em Engenharia Elétrica da Pontifícia Universidade Católica do Rio Grande do Sul.

DRA. LETÍCIA MARIA BOLZANI POEHLS - ORIENTADORA

BANCA EXAMINADORA

DR. VICTOR CHAMPAC VILELA - ELECTRÓNICA - NATIONAL INSTITUTE FOR ASTROPHYSICS, OPTICS AND ELECTRONICS

DR. FABIAN LUIS VARGAS - PPGEE - FENG - PUCRS

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Abstract

Miniaturization has been the industry's main goal over the last few years, as it brings benefits such as high performance and on-chip integration as well as power consumption reduction. Alongside the constant scale-down of Integrated Circuits (ICs) technology, the increasing need to store more and more information has resulted in the fact that Static Random Access Memories (SRAMs) occupy great part of Systems-on-Chip (SoCs).

The constant evolution of nanotechnology brought many revolutions to semiconductors, making it also necessary to improve the integrated circuit manufacturing process. Therefore, the use of new, complex processing steps, materials, and technology has become necessary.

The technology-shrinking objective adopted by the semiconductor industry promoted research for technologies to replace CMOS transistors. FinFET transistors, due to their superior electrical properties, have emerged as the technology most probably to be adopted by the industry.

However, one of the most critical downsides of technology scaling is related to the non-determinism of device's electrical parameters due to process variation. Miniaturization has led to the development of new types of manufacturing defects that may affect IC reliability and cause yield loss.

With the production of FinFET-based memories, there is a concern regarding embedded memory test and repair, because fault models and test algorithms used for memories based on conventional planar technology may not be sufficient to cover all possible defects in multi-gate memories. New faults that are specific to FinFETs may exist, therefore, current test solutions, which rely on operations executing specific patterns and other stressing conditions, may not stand to be reliable tools for investigating those faults.

In this context, this work proposes a hardware-based methodology for testing memories implemented using FinFET technology that monitors aspects of the memory array and creates output signals deriving from the behavior of these characteristics. Sensors monitor the circuit's parameters and upon changes from their idle values, create pulses that represent such variations. These pulses are modulated applying the pulse width modulation techniques. As resistive defects alter current consumption and bit line voltages, cells affected by resistive defects present altered modulated signals, validating the proposed methodology and allowing the detection of these defects. This further allows to increase the yield after manufacturing and circuit reliability during its lifetime. Considering how FinFET technology has evolved and the likelihood that ordinary applications will employ FinFET-based circuits in the future, the development of techniques to ensure circuit reliability has become a major concern.

The presented hardware-based methodology, which was implemented using On-Chip Sensors, has been divided in two approaches: monitoring current consumption and monitoring the voltage level of bit lines. Each approach has been validated by injecting a total of 12 resistive defects, and evaluated considering different operation temperatures and the impact of process variation.

Key-words: FinFET. SRAM. Resistive Defects. Process Variation.

Resumo

Miniaturização tem sido adotada como o principal objetivo da indústria de Circuitos Integrados (CIs) nos últimos anos, uma vez que agrega muitos benefícios tais como desempenho, maior densidade, e baixo consumo de energia. Junto com a miniaturização da tecnologia CMOS, o aumento na quantidade de dados a serem armazenados no chip causaram a ampliação do espaço ocupado por memórias do tipo *Static Random-Access Memory* (SRAM) em *System-on-Chips* (SoCs).

Tal miniaturização e evolução da nanotecnologia proporcionou muitas revoluções na indústria de semicondutores, tornando necessário também a melhoria no processo de fabricação de CIs. Devido a sensibilidade causada pela miniaturização e pelas variabilidades de processo de fabricação, eventuais defeitos introduzidos durante fabricação podem danificar o CI, afetando o nível de confiabilidade do CI e causando perdas no rendimento por *die* fabricado.

A miniaturização adotada pela indústria de semicondutores impulsionou a pesquisa de novas tecnologias visando a substituição de transistores do tipo CMOS. Transistores FinFETs, devido a suas propriedades elétricas superiores, emergiram como a tecnologia a ser adotada pela indústria.

Com a fabricação de memórias utilizando a tecnologia FinFET, surge a preocupação com testes de memória, uma vez que modelos de falhas e metodologias de teste utilizados para tecnologias planares podem não ser suficientes para detectarem todos os defeitos presented em tecnologias *multi-gate*. Uma vez que esta nova tecnologia pode ser afetada por novos tipos de falhas, testes que dependem da execução de operações, métodos de endereçamento, checagem de padrões, e outros tipos de condições de estímulo, podem deixar de serem estratégias confiáveis para o teste dos mesmos.

Neste contexto, este trabalho de mestrado propõe uma metodologia baseada em hardware para testar memórias em FinFET que monitore parâmetros do bloco de memória e gere sinais baseados nessas características. Através do uso de sensores que monitoram os parâmetros do circuito (como consumo de corrente, tensão nas *bit lines*) e detectam mudanças dos padrões monitorados, os sensores criam pulsos que representam essas variações. Esses pulsos são modulados usando técnicas de modulação. Uma vez que defeitos resistivos alteram os parâmetros monitorados, células afetadas por esses defeitos apresentam diferentes sinais modulados, validando a metodologia proposta e permitindo a detecção destes defeitos e consequentemente aumentando o *yield* de fabricação e a confiabilidade do circuito ao longo da sua vida.

A metodologia baseada em hardware proposta neste trabalho foi implementada utilizando sensores integrados no próprio CI, e foi dividida em duas abordagens: monitoramento de consumo de corrente e monitoramento da tensão nas *bit lines*. Cada abordagem foi validada com a injeção de 12 defeitos resistivos de diferentes naturezas e localizações, a após validados considerando diferentes temperaturas de operação e o impacto da variação de processo de fabricação.

Palavras-chaves: FinFET. Memórias SRAM. Defeitos Resistivos. Processo de Variação.

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List of abbreviations and acronyms

IC	Integrated Circuit
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor
CMOS	Complementary Metal-Oxide Semiconductor
SRAM	Static Random Access Memory
SoC	System-on-Chip
PV	Process Variation
SOI	Silicon-over-Insulator
L	Gate Length
T_{OX}	Gate Oxide Thickness
W	Gate Width
V_{TH}	Threshold Voltage
SCE	Short Channel Effects
I_{on}	On-State Drive Current
BOX	Buried Oxide
TG	Tied-Gate
SG	Shorted-Gate
IG	Independent-Gate
H_{FIN}	Fin's Height
T_{FIN}	Fin's Width
T_{BOX}	Buried Oxide Thickness
W_{eff}	Effective Width
V_{DD}	Supply Voltage
DIBL	Drain-Induced Barrier Lowering

BIST	Built-In Self Test
OCCS	On-Chip Current Sensor
SNM	Static Noise Margin
WL	Word Line
BL	Bit Line
GOS	Gate Oxide Shorts
SOF	Stuck-Open Faults
HP	High Performance
MG	Multi-Gate
RNM	Read Noise Margin
RB	Resistive-Bridge
RO	Resistive-Open
TF	Transition Fault
RDF	Read Destructive Fault
dRDF	dynamic Read Destructive Fault
DRDF	Deceptive Read Destructive Fault
dDRDF	dynamic Deceptive Read Destructive Fault
WRF	Weak Read Fault
NSF	No Store Fault
SAF	Stuck-at Fault
CFds	Disturb Coupling Fault
CFrd	Read Disturb Coupling Fault
dCFrd	Dynamic Read Disturb Coupling Fault
LP	Low Power
PWM	Pulse Width Modulation
w1	Write ‘1’

w0	Write ‘0’
SEU	Single Event Upset
NBTI	Negative Bias Temperature Analysis
CC	Current Consumption

Contents

1 Introduction

Miniaturization has been the Integrated Circuit (IC) industry's main goal for the last few years, as it brings many benefits such as high performance and on-chip integration as well as power consumption reduction. By focusing on achieving smaller systems, the IC manufacturing process has undergone many improvements. With these improvements, increasing chip density was possible and has allowed more transistors on a single die.

However, this miniaturization also presented many challenges on conventional planar MOSFET transistors, such as the ones based on Complementary Metal-Oxide Semiconductor (CMOS) technology. Because of the growing leakage and short-channels problems of this technology, it is not possible to shrink this technology below 20nm (HARUTYUNYAN; TSHAGHARYAN; ZORIAN, 2015a) and continue with Moore's Law. Thus, due to its improved short channels and electrostatic characteristics, and design flexibility (VILLACORTA; SEGURA; CHAMPAC, 2016), the FinFET technology has become the most promising approach to continue CMOS scaling and fulfill the requirements of high performance demanded by the shrinking of devices, known as *More Moore* (HEINIG et al., 2014).

FinFETs transistors are studied since 1999, and were first described as non-planar, double-gate transistors (HUANG et al., 1999). According to (WANN et al., 1996), multi-gate transistors showed great potential when compared to other device structures studied, and thus were considered the most attractive device to succeed the planar CMOS transistors when the latter cannot be scaled any further.

Alongside the constant scale-down of IC technology, the increase of data needed to be stored led to a rise in the space occupied by Static Random Access Memories (SRAMs) in System-on-Chips (SoCs). Around 90% of silicon space is already dedicated to SRAMs (International Technology Roadmap for Semiconductors, 2013), thus making memories the most common element on chips. This brings special attention to identify methodical approaches that optimize them.

Technology scaling forces the manufacturing process to be more and more meticulously detailed, making Process Variation (PV) inevitable. It is impossible to assure that all chips will have exactly the same parameters, even if they are on the same wafer. Even though the vendor may guarantee parameters within certain limits, simple variations are a fact in any manufacturing process (WOLF, 1994). Those variations can affect chip reliability, since they can produce different defects, which can have a long-term impact on IC reliability.

This way, this work presents a study of the impact of resistive defects on SRAM

blocks designed using FinFET transistors. Faults models composed of static and dynamic faults are characterized according to the defect type. A hardware-based methodology that aims to monitor signals and generate distinct outputs in the presence of defects is proposed, validated and evaluated in different aspects, such as performance, impact on faulty behavior, temperature, and PV.

1.1 Motivation

FinFET circuits are a relatively new approach to continue the scaling of ICs and fulfill the performance requirements established by the miniaturization-oriented goals of *More Moore* (HEINIG et al., 2014). Currently, only a few foundries are manufacturing circuits based on FinFET technology. This creates a lack of scientific and technical knowledge about critical aspects of FinFET transistors.

Little is known about the impact of manufacturing defects such as resistive-open and resistive-bridge on FinFET-based SRAM cells. Few studies that address such topics have been published, and a full understanding of the subject is still not possible.

In order to improve the set of information concerning FinFET-Based memories reliability and to explore new concepts and the suitability of already proposed ideas when applied to FinFET technology, this work proposes an investigation of several operation aspects of FinFET-based SRAM arrays and test methodologies to identify discrepancies caused by resistive defects.

Considering how far this technology has evolved and the likelihood that FinFET-based circuits will be more and more used in other applications than just rather state of the art applications in the future, it becomes crucial to have a more in-depth knowledge of this technology.

1.2 Objectives

This master's thesis aimed to develop a hardware-based methodology able to identify discrepancies in the behavior of selected parameters of FinFET-based SRAM arrays that may have suffered from manufacture defects. In the current industry's scenario, ICs affected by defects (and specially those defects that do not cause any logical fault) represent one of the main concerns regarding reliability as this issue is becoming more and more common due to miniaturization. Thus, new methodologies that can improve circuit's reliability are essential.

Thus, the following specific objectives have been identified:

- Contextualize the FinFET technology, addressing its main characteristics;

- Analyze the main aspects of a memory array designed with FinFET transistors;
- Establish and characterize a set of resistive defects that may pose reliability issues to FinFET memory cells;
- Perform a fault mapping to identify dynamic fault behaviors and critical resistances for each resistive defect;
- Propose a hardware-based methodology that can be used in manufacturing tests to identify the presence of resistive defects;
- Validate and evaluate the proposed hardware-based methodology regarding impact on faulty behavior, different temperatures of operation, area and power overhead, and PV.

1.3 Methodology

Initially, an extensive research was conducted in order to assure full understanding of all aspects that were discussed in this work. Scientific works and publications related to FinFET technologies, SRAMs, fault modeling, manufacturing defects, PV, and test methodologies were analyzed and used as background.

Then, electric models of FinFET-based memory cells and peripherals were designed. Resistive defects were modeled and injected into these cells and simulated in HSPICE 2014 in order to fully understand the impact of each defect on the behavior of the adopted memory array.

On-chip current sensors were then designed with the purpose to generate output signals that could be used to identify the existence of resistive defects. These sensors were embedded in the memory and their behavior was validated.

Finally, an extensive evaluation was carried out. The behavior in different operation temperatures was investigated. Power consumption during operations and area overhead considering the physical characteristics of transistors were analyzed. Monte Carlo simulations were used to analyze the impact of PV on the output of sensors. At last, a comparison was drawn between both approaches presented in this work.

1.4 Organization

This work was divided in 6 Chapters. In Chapter 1, an introduction is presented. Chapter 2 presents a background of the main concepts addressed in this work. FinFET Technology, PV, SRAMs, Resistive defects, fault modeling, and test methodologies are discussed.

Chapter 3 presents the proposed technique of this work. A characterization of the designed memory array is presented, and the specification and implementation of the hardware-based approach is laid out.

Chapter 4 presents the validation of the memory array and the sensors implemented. The experimental setup used in all simulations is defined, and first results are introduced. In Chapter 5, evaluations are carried out. Discussions regarding the impact of temperature, overheads, and PV are presented.

In Chapter 6, results obtained during evaluations are summarized and compared. Conclusions regarding mains aspects of the proposed hardware-based approach are drawn. In the end, possible future works within the scope of this thesis are discussed.

2 Background

Difficulties emerged due to the constant evolution and miniaturization of CMOS technology were promptly resolved and settled by improving manufacturing capabilities, allowing a substantial improvement in the industry of semiconductors and ICs.

However, miniaturization has become more and more challenging as manufacturing is reaching the materials' physical limitations. For a device length (L) of less than 100nm, saturation velocity and source velocity limit provide limited improvements in performance (LUNDSTROM, 1997). Miniaturization of the thickness of the gate dielectric (T_{OX}) is also a concern. Below 1.2nm, quantum mechanical tunneling current from the gate into the channel becomes significant (MINAYA, 2014), and further reductions in T_{OX} may result in large static leakage current and large power consumption, even in the case that the device is turned off.

The manufacturing process is also approaching the equipament's limit. Technology scaling forces the manufacturing process to be more and more detailed, making PV inevitable. It is impossible to assure that all chips will have exactly the same parameters, even if they are on the same wafer. Even though the vendor may guarantee parameters within certain limits, simple variations are a fact in any manufacturing process (WOLF, 1994). These fluctuations in the manufacturing process represent variations on many parameters, such as gate length (L), gate width (W), gate oxide thickness (T_{OX}), and threshold voltage (V_{TH}), and are caused mainly due to sub-wavelength lithography and random dopant fluctuations. As technology shrinks, these variations start to pose a challenge in the manufacturing process' yield and circuit's reliability. Thus, new approaches are needed to allow future technology miniaturization. Multi-gate structures, such as the FinFET technology, are a promising approach.

2.1 FinFET Technology

Multi-gate devices have many advantages that have been studied and demonstrated in FinFET technologies for the past decade (Fu-Liang Yang et al., 2002; ARNIM et al., 2007). Of all, the main advantage of this technology is the improved short channel effects (SCE) due to the electrostatic control of the channel made on multiple sides by the gate, which provides a better control than standard transistor structures, such as CMOS. This allows a better leakage current control, opening up the possibility for even smaller transistor and boosting even further technology's miniaturization.

A second advantage of these devices is the improved circuit speed due to a refined

on-state drive current (I_{on}). By reducing channel doping, the electric field normal to the SiO_2 is minimized, which therefore reduces the surface roughness scattering. The state drive current can be improved even more by the FinFET technology, as it provides a larger channel width with a small footprint area; this raises I_{on} even more, and proves to be useful for driving large capacitive loads, such as in interconnects (MINAYA, 2014).

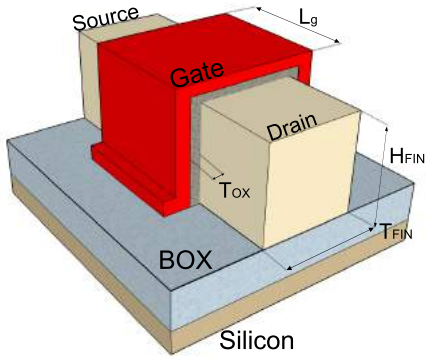
Finally, a last advantage of this new technology is the reduced manufacturing variation due to the absence of channel dopants, minimizing the effect of random dopant fluctuation. However, although minimized, PV may still cause reliability issues on the device, as shown by Harutyunyan (HARUTYUNYAN; TSHAGHARYAN; ZORIAN, 2015a).

FinFET is the denomination of one of the most feasible multi-gate structures. It consists of thin, vertical slices of silicon – known as fins – that are wrapped around by the gate, and placed on top of oxide. There are many ways to construct a FinFET transistor, and each way results in a different final product (DESHMUKH et al., 2015). In Silicon-over-Insulator (SOI) FinFETs, fins are built over buried oxide (BOX) and are isolated from the substrate. In Bulk FinFETs, the fin is connected directly to the substrate through the oxide layer, and a Shallow Trench Isolation (STI) of oxide is formed on the side. There is also different gate configurations. In Tied-gate (TG) FinFETs, or as it is also called Shorted-Gate (SG) (LIU; XU, 2012), there is only one gate, and it covers the fin from all three sides. Another model is the Independent-gate (IG) FinFET, which has two gates (on front and back sides) that are controlled separately and are independent from each other (HARUTYUNYAN et al., 2014). However, most of the leading IC manufacturing companies, such as Intel and Samsung, produce mainly TG FinFETS as shown in (Samsung Semiconductor, 2013; INTEL, 2011). Consequently, the majority of research done so far focuses mostly on TG FinFETs. Fig. 1 illustrates the differences of SOI and Bulk TG FinFETs and their parameters, while Fig. 2 pictures schematic representations of both TG and IG models.

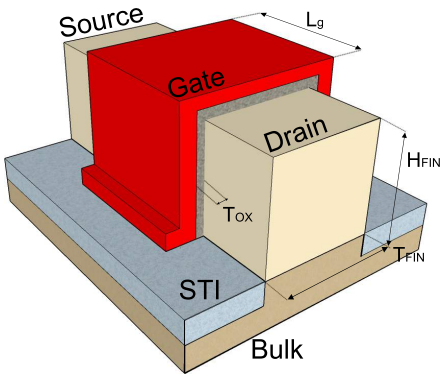
The most important parameters of a FinFET transistor are its fin's height (H_{FIN}) and width (T_{FIN}), and its channel length (L) (HARUTYUNYAN; TSHAGHARYAN; ZORIAN, 2015b). Other parameters, such as gate oxide thickness (T_{OX}), buried oxide thickness (T_{BOX}), body doping, gate/source doping supply voltage, among others, complete the typical parameters of a FinFET transistor (SIMSIR; BHOJ; JHA, 2010).

As the gate of a FinFET transistor wraps around the silicon fin, this creates three distinct channel sides – two on the side, and one on the top. Thus, another important feature of this transistor is that current flows along the top and lateral covering of the fin. This way, it is possible to define the effective channel width as W_{eff} = (2 x H_{FIN} + T_{FIN}) x NFIN, where NFIN is the number of fins on the transistor. Fig. 3 shows the current flow on a FinFET, represented by the yellow arrows.

Height and width of fins determine the operation of the device. By increasing



(a) SOI FinFET.



(b) Bulk FinFET.

Figure 1: Tied-Gate FinFET structure, and its parameters.

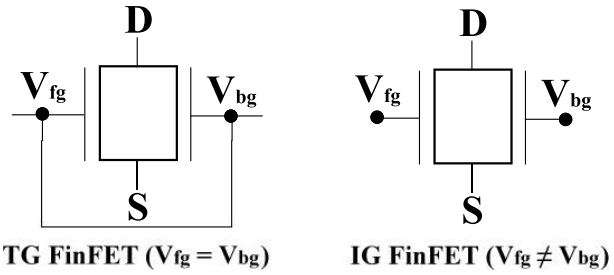


Figure 2: Schematic representations of Tied-Gate and Independent-Gate FinFETs.

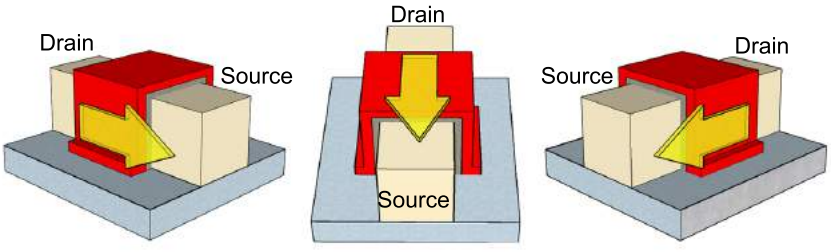


Figure 3: FinFET Current flow.

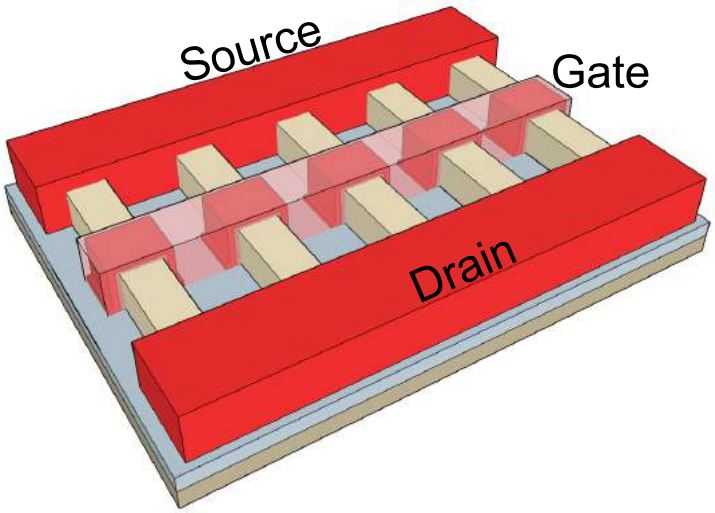


Figure 4: A five fin FinFET transistor.

width, the transistor starts to behave as a planar structure. Shrinking the width is not a problem, as the lateral gates can provide excellent control, not only reducing short channel effects, but also allowing the growing of a thicker layer of gate oxide compared to planar structures, which reduces gate tunneling leakage current and improves the drive current of the FinFET device (MINAYA, 2014). However, once the height and width of a fin are fixed, the only way to change W_{eff} and increase the channel's current drive capability is by using more fins. Fig. 4 depicts a FinFET transistor composed of five fins.

The manufacturing process of planar structures is not much different from FinFET structures. Conventional lithography and etch processes can be used to pattern and construct transistor's gates. However, fins construction requires specific steps and handling. Traditionally, the industry utilizes a technique denominated Fin-First Process (Yang-Kyu Choi; Tsu-Jae King; Chenming Hu, 2002) where the fin is the first structure built on the wafer. An alternative approach, known as Fin-Last Process (CHANG et al., 2011), can also be utilized. In this process, the fin pattern is transferred to the underlying silicon only at the end of manufacturing, when the dummy gate used during fabrication is removed.

2.2 Process Variation

With the consistent miniaturization of technology, the process of manufacturing is working with materials at their physical limit. In such small scale (less than a hundred nanometers), it is impossible to assure perfection. Such imperfections affect transistor's main parameters that will define the behavior of the IC, like gate length (L), gate width (W), gate oxide thickness (T_{OX}), threshold voltage (V_{TH}), etc. There are many causes for process variations, but its main sources are Sub-wavelength Lithography, material deposition and planarization, and dopant implantation (MINAYA, 2014).

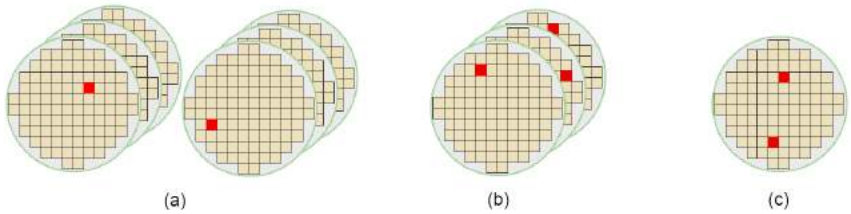


Figure 5: PV affecting multiple dies.

In older technologies, a process called Photo-lithography was used to draw structures on the wafer, as the size of transistors was not so small. However, in nanometer technologies, where transistors are smaller than the wavelength of light, the lithography process must be able to print such small measures. Thus, a more developed process, called Sub-wavelength Lithography, was created. Even though this process can print smaller patterns, this new process suffers from distortions caused by optical interference and diffraction, and it is expected that as technologies shrink, the variations caused by lithographic deviations will be larger. Line width variation, corner rounding, line-end shortening, and line-edge roughness are the main types of distortions due to lithography.

During manufacturing, there are many stages where materials are deposited on the wafer or removed from it. During these stages, it is not possible to assure that, for example, all areas of the chip will be polished at the same pace. Such inconsistencies are the main cause of dishing and erosion phenomena.

Dopant implantation is the process of inserting dopant atoms into the transistor's substrate. With smaller technologies, fewer atoms are implanted, and the process of implanting it has a random behavior. Thus, such fluctuations may cause variations in transistors' V_{TH}.

Process Variations are usually divided into two groups: systematic and non-systematic. Variations that are known and can be determined before manufacturing are denominated systematic PV. During the process of back-end, after layout is finished, it is possible to measure and model these variations with fixed values and estimate the impact of these variation on the circuit's performance.

If it is not possible to determine variations before manufacturing, then such variations are denominated non-systematic. They are due to the inaccuracy of the control process. They can be partitioned into Inter-Die Variations, if the variation is perceived equally throughout the entire die, or Intra-Die Variations, if each device or interconnection in a die is affected in a different way. Fig. 5 illustrates the differences between Inter-Die variations. Lot-to-Lot (Fig. 5.a) variations are characterized by inconsistencies between batches of wafers, Wafer-to-Wafer (Fig. 5.b) by variations between wafers of the same lot, and Die-to-Die (Fig. 5.c) between dies in a same wafer.

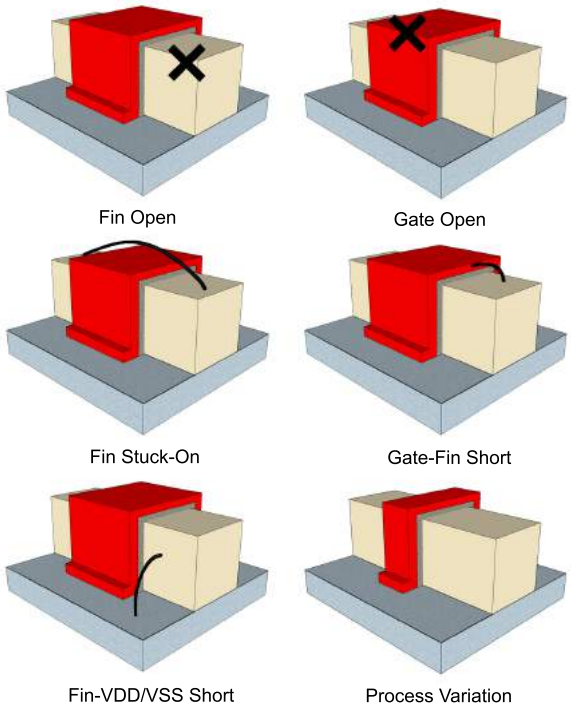


Figure 6: FinFET-specific defects.

2.3 Process Variation on FinFET based circuits

The impact of PV on FinFET transistors is not fully known . However, when compared to planar-based memories, FinFET-based memories proved to be more stable to PV faults. While changes of 20% to 40% in parameters size are enough to sensitize different types of faults in memories based on CMOS technology, for example, changes below 50% in parameters do not lead to any fault in FinFET-based memories (HARUTYUNYAN et al., 2013). It was defined in (HARUTYUNYAN; TSHAGHARYAN; ZORIAN, 2015b; HARUTYUNYAN; TSHAGHARYAN; ZORIAN, 2015a; HARUTYUNYAN et al., 2014) some of the possible altercations on FinFET transistors due to PV, which are illustrated in Fig. 6.

It is important to note that those defects shown in Fig. 6 are specific to FinFET devices. When considering other structures, one should also consider defects that are typical to planar-based structures; in memories structures, there are other defects that may affect reliability, such as resistive-bridges (RBs) between word and bit lines, resistive-opens (ROs) in the peripherals around the memory array, among others.

2.4 Static Random Access Memories

Static Random Access Memories (SRAMs) are composed of cells designed to store logic values that can be retained at any time by using flip-flops. This kind of memory is

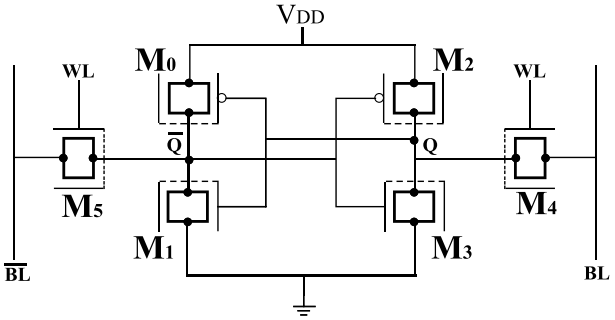


Figure 7: 6T FinFET SRAM Cell Schematic.

referred as static because it does not require periodic refresh signals in order to preserve their stored data (WOLF, 1990). There are many types of SRAM cells, and they are designed to be as small as possible to allow a higher density. However, many reliability aspects impose certain sizing restrictions (RABAEY, 1996).

When considering state-of-the-art memories, there are many factors that prevent further scaling down and improvements. One of the main concerns is the power consumption. Lowering the supply voltage (V_{DD}) proves to be the best alternative to save power. Yet, conventional CMOS SRAMs are limited to miniaturization due to the random variations of threshold voltage (V_{TH}) caused by Random Dopant Fluctuation. As high doping is not required in FinFETs owing to their enhanced SCE effects, Random Dopant Fluctuation is expressively reduced, which diminishes V_{TH} variations and allows V_{DD} to be scaled down.

Further, FinFET technology can bring many specific advantages to SRAM memories' performance and stability. Improved sub-threshold swing allows not only lower V_{TH} for a given off-state leakage current, but also enhances the on-state current per device width. Such improvement shortens the read and write access times on FinFET SRAM cells. Furthermore, the less-relevant drain-induced barrier lowering (DIBL) effects in this technology induces to smaller output conductance ($\partial I_D/\partial V_{DS}$) in the saturation region, leading to sharper voltage transfer characteristics, improving the read Static Noise Margin (SNM) of FinFET SRAM cells.

One of the most important models of SRAM cells is the design based on six transistors (6T), which is represented in Fig. 7. The 6T memory cell consists of two pass transistors that are shared between read and write operations, and four other transistors that represent two cross-coupled inverters. The word line (WL) replaces the clock and controls the transistors M5 and M6 (pass transistors) that are connected each to their respective bit line (BL). The value stored in the cell corresponds to the ΔV between inverters (M1 & M2, M3 & M4).

Jointly, a group of SRAM cells forms a matrix structure, allowing data storage in any combination of rows and columns. All cells share electrical connections: vertically,

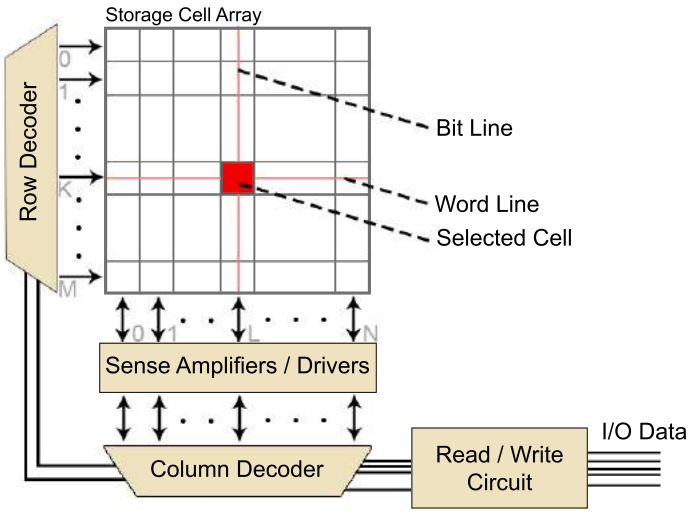


Figure 8: SRAM Block consisting of (M+1)x(N+1) cells.

through the bit line, and horizontally, through the word line. Each cell has a unique position (address), so it is possible to access each one of them individually by the appropriate selection of word and bit lines.

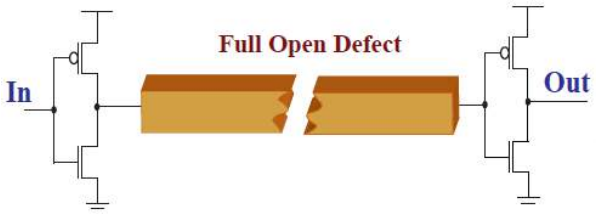
Around the main array of SRAM cells, other circuits guarantee proper operation. There are two *address decoders*: one for the word line (rows), and the other for the bit line (columns). Another circuit is responsible for read and write operations. It can either receive a value and then work the bit lines to store it; or it can read the value already stored on the cell by estimating the ΔV and then output the data retrieved. There are also sense amplifiers for every column; they help by amplifying the signals that are about to be written or were just read. Fig. 8 depicts an example of this architecture.

2.5 Defect, Fault, and Error

Models can serve as abstraction of physical events. Through them, it is possible to analyze such events and finalize solutions. In this context, three fundamental terms are used to express these events – defects, errors, and faults. Many definitions co-relate and establish a cause-effect relationship between them.

According to (BUSHNELL; AGRAWAL, 2013), *defect*, *fault*, and *error* are defined as the following:

- **Defect**: A defect in an electronic system is the unintended difference between the implemented hardware and its intended design;
- **Fault**: A representation of a "defect" at the abstracted function level;



(a) Full open defect.

(b) Resistive open defect.

Figure 9: Difference between Open Defects (MINAYA, 2014).

- **Error**: A wrong output signal produced by a defective system is called an error. An error is an "effect" whose cause is some "defect".

2.6 Resistive Defects

The constant evolution of nanotechnology brought many revolutions to semiconductors, making it also necessary to improve the IC manufacturing process. Therefore, the use of new, complex processing steps and materials are imperative (MINAYA, 2014). Due to the sensitivity caused by the miniaturization of circuits and process variability present during manufacturing, defects introduced throughout the process can impair the chip, affecting IC reliability and causing overall yield loss.

There are many types of defects that can compromise the chip's reliability. In this context, two of them — resistive-open (RO) and resistive-bridge (RB) defects — are described in detail.

2.6.1 Resistive-Open Defects

A resistive-open defect is characterized as a discrepancy in the connection between two nodes. Also known as a weak open defect, they happen during the manufacturing process and are primarily due to imperfections or inconsistency in the process. They are characterized by still maintaining connection between nodes, even though it is compromised. Contrasting the first, *full-open* (or simply *open*) defects are characterized as a disruption in the connection between two nodes. Fig. 9 depicts this difference.

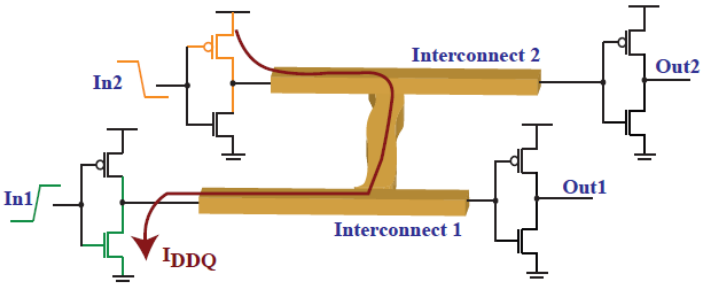


Figure 10: A bridge defect connecting two independent points (MINAYA, 2014)

Concerning the standard 6T design of SRAMs, there is a total of 18 spots where resistive-open defects can occur. The position where a defect occurs directly affects which fault behavior will be observed in the cell. However, due to cell's symmetry, a set of only six defects are already enough to analyze the impact of this type of defect on the cell's performance.

2.6.2 Resistive-Bridge Defects

A resistive-bridge defect creates a connection between two nodes that should have no relation. Like a resistive-open defect, its main causes are inconsistencies and imperfections in the manufacturing process. This new connection has a fixed resistance value that depends on its shape and the materials involved.

Resistive-Bridge defects detection may be not trivial. If the resistance of the new connection is sufficiently small, the circuit will be affected by a delay large enough to cause failures, which can be detected by traditional test methods. Nevertheless, if the resistance is not significantly small, the delay induced will not be large, thus causing the defect not to be detected as it will not produce a fault. This may represent an issue in IC reliability (DILILLO et al., 2005). Fig. 10 depicts a new connection in a circuit, illustrating the concept of resistive-bridge defects.

The impact of this type of defect on 6T SRAM cells depends on the location of the defect and the resistance of the new connection as well. High resistance connections usually cause weak read faults, while low resistance connections tends to cause stuck-at faults (FONSECA et al., 2010).

2.7 Fault Modeling

Fault modeling is the representation of faulty behaviors and patterns in a circuit. It is of utmost importance when talking about circuit testing and test effectiveness that fault models accurately reflect the behavior of defects. The impact of those defects on the

circuit must be completely understood, as they are responsible for producing the output errors in order for the fault to be detected (STROUD, 2002).

According to (HAMDIOUI et al., 2004), there are two classes of faults. The first, denominated *static faults*, are faults that can be perceived with a single operation; e. g. a single read operation in the cell would be enough to detect a fault in the output. This class was enough to represent all models of fault in old technologies.

However, with miniaturization, another class of faults emerged, denominated *dynamic faults*. This behavior requires a sequence of at least two operations to be sensitized; e.g., a write operation followed by a sequence of read operations. A write or read operation alone in the cell would not detect any fault; yet, after a write operation immediately followed by n read operations, a faulty behavior is detected.

Concerning memory cells affected by resistive defects, different types of defects and their spot can provoke different faults. The definitions of most faults used in this work are the following, as described by (FONSECA et al., 2010; DILILLO et al., 2005):

- **Transition Fault (TF)**: A cell is said to have a TF when it fails to flip the value stored (0 to 1 or 1 to 0);
- **Read Destructive Fault (RDF)**: A cell is said to have an RDF when a read operation on the cell causes the value stored to flip, outputting the wrong data;
- **dynamic Read Destructive Fault (dRDF)**: A cell is said to have a dRDF when a read operation, after n other successful read operations, changes the value stored, outputting the wrong data;
- **Deceptive Read Destructive Fault (DRDF)**: A cell is said to have a DRDF when a read operation on the cell outputs the correct value, but then changes the value stored;
- **dynamic Deceptive Read Destructive Fault (dDRDF)**: The dynamic behavior of DRDF. A cell is said to have a dDRDF when, after n successful read operations, the following read operation flips the value in the cell, even though the output data is correct;
- **Weak Read Fault (WRF)**: A cell is said to have a WRF when during a read operation, the ΔV between bit lines BL and $\overline{BL}$ is not enough for the sense amplifier to produce the correct logic output;
- **No Store Fault (NSF)**: A cell is said to have a NSF when it cannot retain a logical value;

- **Stuck-at Fault (SAF)**: A cell is said to have a SAF when it is unable to store both logic values. Stuck-at 1 represents a cell that cannot store logical value '0', while Stuck-at 0 represents the opposite.
- **Disturb Coupling Fault (CFds)**: This fault affects a group of at least two cells, and is sensitized when a read or write operation in one cell affects another cell or group of cells, forcing them to change their value stored.
- **Read Disturb Coupling Fault (CFrd)**: This fault occurs when a read operation performed on a defect-free cell changes the data in the cell and returns the incorrect value on the output if a given value is present in a defective cell.

According to (HARUTYUNYAN; TSHAGHARYAN; ZORIAN, 2015a), Dynamic faults became even more relevant in FinFET-based devices. As technology shrinks, the probability of dynamic faults in FinFET-based devices is much higher when compared to planar-based devices, which proves the necessity of test methodologies and strategies adapted to detect this specific class of faults.

2.8 Test Methodologies

Test methodologies are essential to assure the quality and functionality of manufactured circuits. Different methodologies differ from what is tested, what is monitored, and how it is monitored. This section presents three classic methodologies already adopted by the industry in planar technologies, which are essential to the proposed test methodology that will be presented and discussed in the following chapters.

2.8.1 March Test

March Test is a memory-specific test methodology adopted alongside Built-In Self Test (BIST). It executes access operations algorithms aiming to sensitize functional faults for detection, assuming that by writing a value in a cell, it is expected to read the same value. March Tests are used with embedded controllers that manage the execution of operations and the reconfiguration of the memory when defective rows or columns are detected, when recuperation techniques are present (LI; TSENG; HOU, 2010).

This methodology is very useful in detecting static faults. And as the nature of the test enforces a small number of operations per cell, it becomes a great option for manufacturing test. Several algorithms have already been proposed to detect static memory faults. The algorithm proposed in (HAMDIOUI; GOOR; RODGERS, 2002), known as *March SS* and presented in Algorithm 1, became one of the most used algorithms as it executes only 22 operations per cell and claims to detect all functional faults among individual cells and linked faults (e.g. coupling faults) between maximum two cells.

First, the algorithm ensures that the value '0' is written in all the memory's cells, regardless of the direction (increasing or decreasing the address of access) of execution. Then, in decreasing address order, the algorithm evaluates each cell's capabilities regarding the value '0'. The algorithm resets the address, and in the same manner evaluates the cells' capabilities to store the value '1'. The algorithm repeats these two evaluations, but now increasing the address. Finally, the algorithm read all cells, expecting to read the last value of '0' previously written.

Algorithm 1 March SS

$\Updownarrow (w0);$
$\Uparrow (r0, r0, w0, r0, w1); \Uparrow (r1, r1, w1, r1, w0);$
$\Downarrow (r0, r0, w0, r0, w1); \Downarrow (r1, r1, w1, r1, w0);$
$\Updownarrow (r0)$

For the detection of dynamic faults, other algorithms for March Test have been designed, as in (HAMDIOUI et al., 2003; HARUTUNYAN; VARDANIAN; ZORIAN, 2006). However, most of the approaches can only detect dynamic faults within a range of two operations, or need to execute a great number of operations (around 70) in each cell of the array. This way, March Test becomes a poor solution to detect dynamic faults.

2.8.2 I_{DDQ} Test

I_{DDQ} Test consists of monitoring current consumption of circuits for diagnosis. Thus, it can be adopted not only in memories, but also in logic circuits. Monitoring happens during the execution of a pre-defined set of inputs, and diagnosis can be achieved through two approaches: first, by comparing the current consumption with defined thresholds; and by comparing current consumption among identical circuits when subjected to same inputs. This approach assumes that the presence of defects or faults will inevitably distort current consumption, thus allowing detection.

However, this test methodology proves to be limited when the complexity of the analysis becomes more realistic. As circuits becomes smaller, PV becomes more and more significant. This way, the distinction between current consumption discrepancies caused by weak defects and the inherent PV present on the monitored circuit becomes problematic.

2.8.3 On-Chip Current Sensor associated to March Test

Akin to I_{DDQ} Test, it is possible to monitor current consumption by using On-Chip Current Sensors (OCCSs).

OCCS are usually composed of two parts: a current to voltage converter, and an operational amplifier. Designing an OCCS may be a difficult task, as challenges in noise

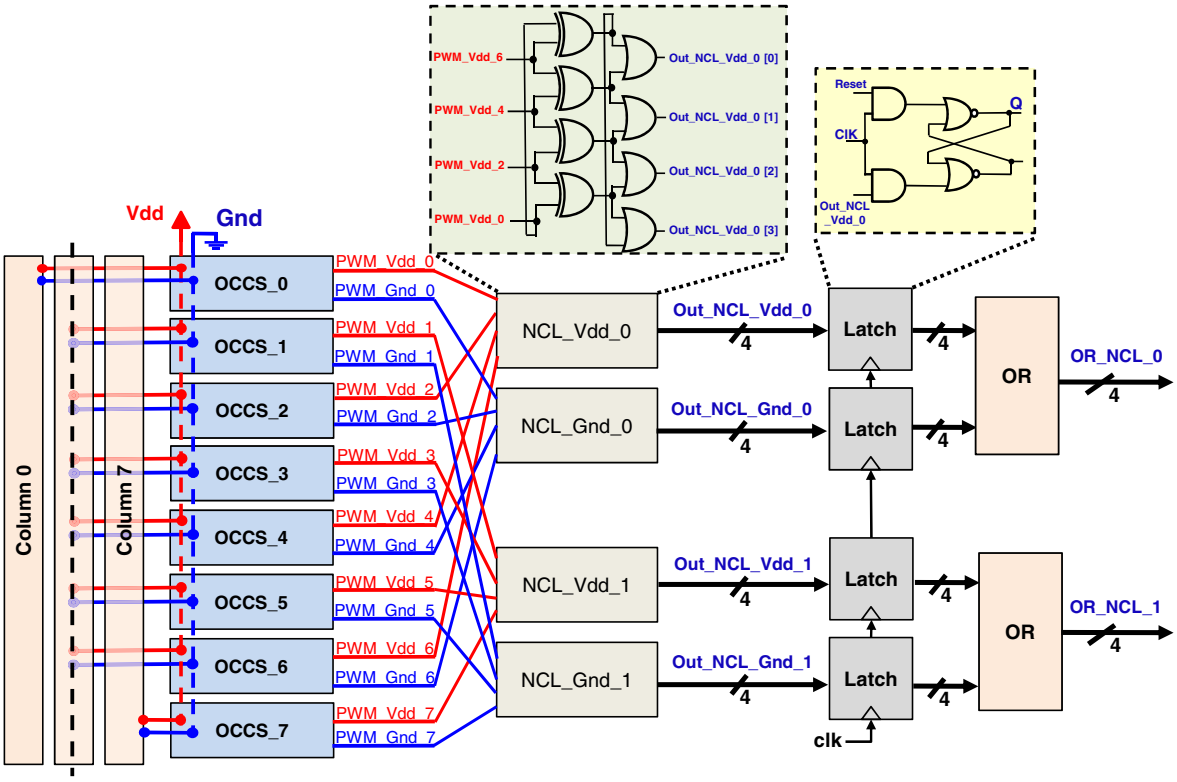


Figure 11: Architecture of the hardware-based approach proposed in (GOMEZ et al., 2016).

aggregation, delay, efficiency, area and power overhead, and PV have a direct "Short Blanket" effect on the sensor efficacy.

OCCSs have been previously adopted to detect defects in CMOS technologies. In (LAVRATTI, 2012; LAVRATTI et al., 2013; LAVRATTI et al., 2015; GOMEZ et al., 2016), the authors proposed the utilization of OCCS alongside a neighborhood comparison logic to detect resistive-open defects in 65nm CMOS technology. The overall architecture of the approach is presented in Fig. 11. The authors used OCCS to compare current consumption of memory cells while performing simultaneous read and write operations. For identical defect-free SRAM cells, the difference between the current consumption waveform should be close to zero. On the other hand, if a defect exist in one of the cells, the difference of its current consumption with respect to a defect-free cell should be different from zero. While the authors successfully proved the use of OCCSs for this matter, a great part of the study was focused on the validation of the detection technique, rather than the evaluation of the efficacy of the sensor to produce valid results.

2.8.4 Challenges on Defect Detection

The challenges presented on previous sections can be enumerated as follow:

1. March Tests are not efficient regarding the detection of dynamic faults that require

more than two operations to sensitize faults;

2. I_{DDQ} Tests, when monitoring the entire circuit current consumption, are not able to distinguish discrepancies caused by PV and discrepancies caused by the presence of resistive defects;

3. Current consumption is directly affect by the defect's size, physical position in the cell's layout, operation frequency, and mode of access (read or write access). Thus, methodologies that use fixed thresholds are not a viable option to detect a wide range set of resistive defects.

   Thus, proposing a test methodology, one should be aware of these aspects and introduce new techniques that are able to overcome the aforementioned challenges.

2.8.5 Test Methodologies for FinFETs

With the production of FinFET-based memories, there is a concern regarding embedded memory test and repair as fault models and test algorithms used for conventional memories (based on planar technology) may not be sufficient to cover all possible defects in multi-gate memories. As there may exist new faults that are specific to FinFETs, existing test solutions that rely on test operations, addressing methods, background patterns, and other stressing conditions may not be reliable tools for investigating those faults (HARUTYUNYAN et al., 2014).

In (LIU; XU, 2012) the authors first showed a study regarding three different types of defects: stuck-on, stuck-open and gate oxide short. To detect defects and faults, they proposed the utilization test vectors for delay comparison, and I_{DDQ} for current comparison. However, they concluded that these methodologies cannot be directly used, and some extra efforts and new strategies to carefully generate new delay fault vectors are necessary.

I_{DDQ} test was also used on (Chen-Wei Lin; CHAO; Chih-Chieh Hsu, 2013) to investigate Gate Oxide Shorts (GOS) on FinFET-based SRAMs. The authors also emphasized the limitations of this methodology for FinFETs, and proposed two new methodologies (one for TG, another for IG) able to spot the GOS defects that were not detected by I_{DDQ}. For TG FinFETs, it is proposed the execution of a write operation while both bit lines are floating. If there is a defect on the cell, the voltage difference between bit lines decreases rapidly due to the GOS induced current, and the write operation fails. For IG FinFETs they also consider the testing of decreased saturation current, and change the voltage of one of the bit lines. This way, it is possible to detect both front-gate and back-gate GOS defects.

A fault detection strategy for stuck-open faults (SOF) was shown in (CHAMPAC et al., 2012; VAZQUEZ et al., 2009). To improve the detection of these faults, the authors

proposed a test vector strategy that aims to produce lower values at the transistor drain-source voltages of fan-out gates. This was due to the reduced hold time caused by increased sub-threshold and gate leakages in transistors with SOF, which turns detection less trivial.

In (HARUTYUNYAN et al., 2014), the authors proposed a new methodology for modeling FinFET-specific faults. Based on that, they developed an automated flow for SPICE simulations, injecting defects into memory layouts and memory SPICE netlists. The main results the authors obtained from this methodology is that FinFET-based memories, compared with planar-based memories, are prone to suffer more from dynamic faults, but less from PV.

3 Proposed Technique

The effects of technology shrinking had severe impacts on manufacturing process of semiconductors. By utilizing photolithography and masks to build transistors and interconnections within the design's physical specifications, many imperfections and inconsistencies started to jeopardize the reliability of ICs. Many of these defects are weak defects, a special type of defects that, due to their low impact on the circuit's output during manufacturing test, are increasing the complexity in defects detection.

Further, with new technologies starting to be adopted by the industry in mass production devices, it is not entirely known if prevailing test methodologies, which are mainly used in planar technologies, are enough to provide satisfactory results. Thus, the development of a new test methodology aimed specifically at FinFET-based devices proves to be necessary.

This thesis proposes a new hardware-based methodology to detect defects, including weak defects, on FinFET-based memories. Different methodologies have been proposed in literature. These methodologies provide detection by monitoring voltage supply between cells or by performing extensive Built-in Self-Tests (BISTs). However, the efficiency of these methodologies is not known regarding FinFET-based circuits. This thesis aims at developing a test methodology for FinFET-based memories.

A Low Power (LP), Multi-Gate (MG) FinFET library of 20nm developed by PTM (Nanoscale Integration and Modeling (NIMO), 2012) that describes Tied-Gate, Bulk Mode FinFETs transistors was adopted. This library was used to describe all circuits and memory peripherals (buffers, decoders, etc.) in SPICE language. Once all circuits were properly described, they were simulated, validated and evaluated.

3.1 FinFET Technology Characterization

The (Nanoscale Integration and Modeling (NIMO), 2012) website maintains a collection of accurate, customizable, and predictive technology models for design and research purposes. They developed a full package for multi-gate transistors consisting of 5 technology nodes (20nm, 16nm, 14nm, 10nm, 7nm) and two different design approaches (High Performance and Low Power). The user also has the option to choose between SOI and Bulk FinFETs. For this work, the 20nm, Low Power, Bulk Mode model was adopted. Its parameters are shown in Table 1. Fig. 12 depicts the DC analysis of the NMOS transistor for different Gate to Source Voltages (V_{GS}). With a V_{GS} of 0.9 V (nominal supply), the Current flowing from Drain to Source (I_{DS}) is approximately 52 μA.

Parameter	Value
Power Supply	0.9 V
Minimum Gate Length (L_{min})	10 nm
Maximum Gate Length (L_{max})	24 nm
T_{FIN}	15 nm
T_{OX}	1.4 nm
H_{FIN}	28 nm
PMOS Mobility ($\mu 0$)	0.026 $cm^2/(V \cdot S)$
NMOS Mobility ($\mu 0$)	0.038 $cm^2/(V \cdot S)$
PMOS Gate Work Function ($PHIG$)	4.6215 eV
PMOS Gate Work Function ($PHIG$)	4.5568 eV

Table 1: PTM 20nm Model Parameters.

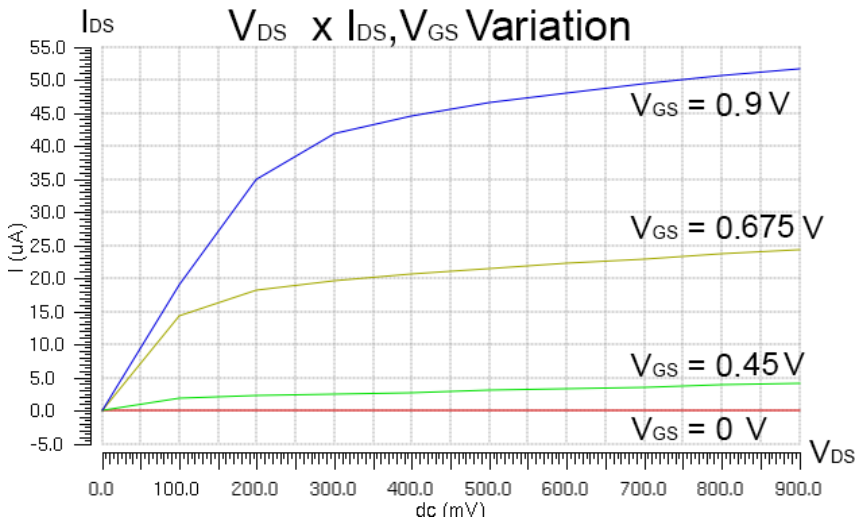


Figure 12: NMOS DC Analysis for different V_{GS}.

The properties of FinFETs transistors designed with different amounts of fins were also evaluated. A linear behavior between I_{DS} and number of fins, proving that I_{DS} and W_{eff} are linearly proportional to the number of fins used to design the transistor, was observed. The current observed on a transistor designed with 5 fins was approximately 260 μA, five times the current observed on a transistor with only one fin. These observations are shown in Fig. 13.

3.2 FinFET SRAM Cell Characterization

To consolidate the proposed methodology for this thesis and analyze defects on FinFET technology, a FinFET-based 6T memory cell was designed following the specification presented on (BURNETT et al., 2014). The cell consists of six FinFET transistors,

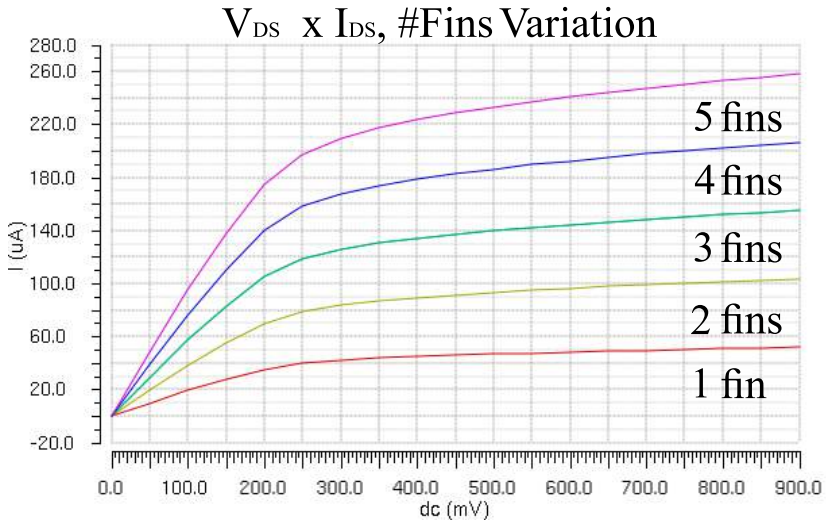


Figure 13: NMOS DC analysis for different configurations.

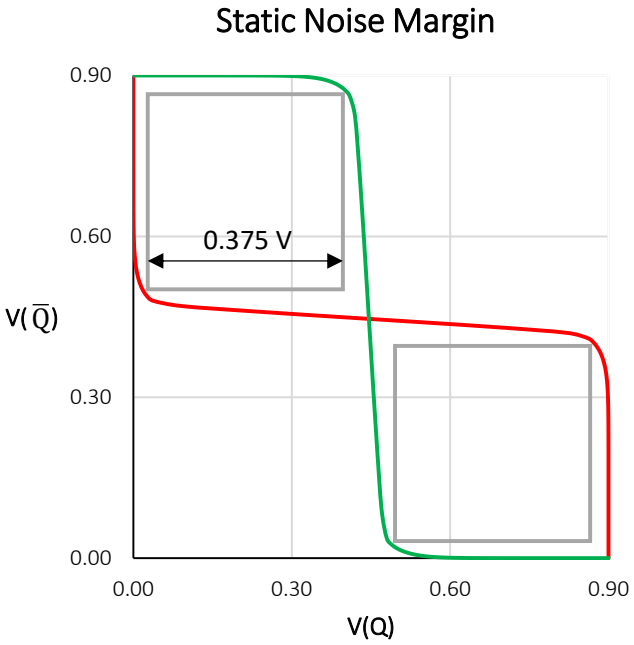


Figure 14: Static Noise Margin.

all designed using only one fin each. This way, cell area can be minimum.

To evaluate the cell's stability regarding external noise, the SNM of the designed cell was measured by plotting the butterfly graph of the output of both inverters, obtained through DC analysis. Then, a square was drawn between both curves, where the SNM is represented as the maximum side length of this square. Fig. 14 show that the SNM measured for this cell is 0.375 V.

Such a symmetric plot was observed due to the symmetry of inverters' pull-up (PU) and pull-down (PD). Both NMOS and PMOS transistors were designed using only one fin. As more fins are used exclusively on the pull-down or on the pull-up, the curve

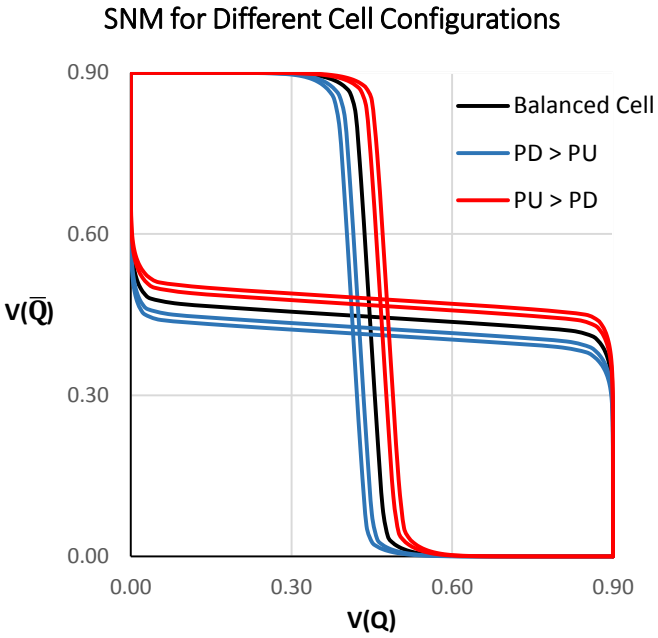


Figure 15: Static Noise Margin for different cell configurations using 2 or 3 fins on PU and PD.

shifts from the center. This behavior is shown in Fig. 15, which shows the SNM of cells designed using more fins on PD (blue curves) and on PU (red curves). Designing PMOS and NMOS transistors with different parameters (such as gate length) also caused shifts in the SNM curve.

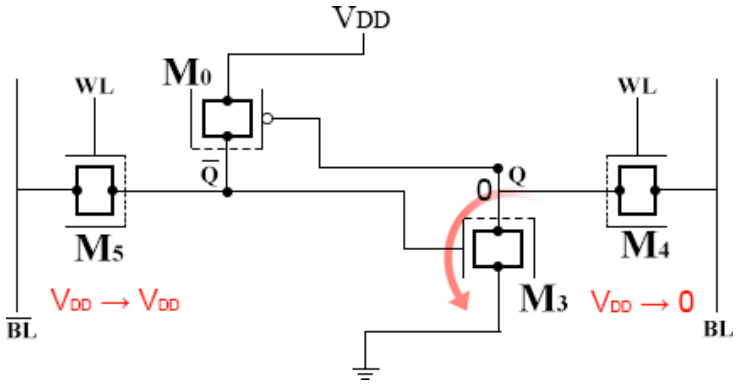
Leakage current, which is the current consumption when the cell is in stand-by mode, was measured by monitoring the current from V_{DD}. Current consumption is roughly 40 pA. Thus, leakage power on the designed cell is approximately 36 pW.

3.2.1 Read Operation

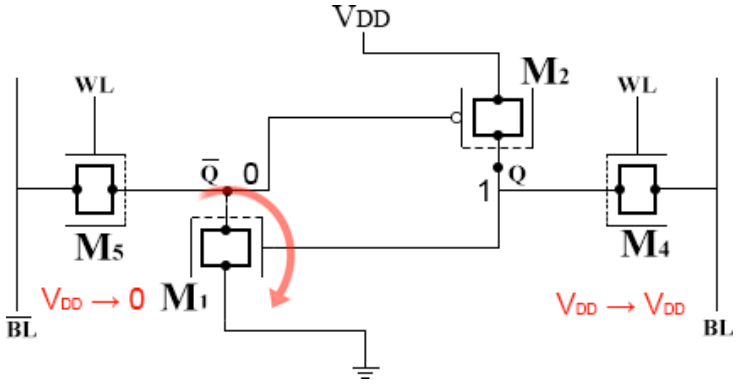
During a correct read operation, both bit lines are pre-charged to V_{DD} and the word line is asserted, thus enabling pass-transistors M4 and M5. The values stored in Q and $\overline{Q}$ are then transferred to the bit lines based on the logic state of the cell.

To perform a read operation, both bit lines must be previously charged to V_{DD}. The read operation starts when the word line signal is activated, enabling pass transistors M4-M5. If the cell is storing a '0' (Q = '0', $\overline{Q}$ = '1'), the value at $\overline{BL}$ is not altered, while BL is discharged through M4–M3. However, if the cell holds a logic value of '1' (Q = '1', $\overline{Q}$ = '0') then the opposite occurs, with $\overline{BL}$ being discharged through M5-M1 while BL remains high. Fig. 16 illustrates both cases, while Fig. 17 shows a simulation example of the Read '1' Operation.

During read operations, the cell becomes more vulnerable as it is being accessed



(a) Read '0' Operation.



(b) Read '1' Operation.

Figure 16: Read Operations on a 6T SRAM Cell.

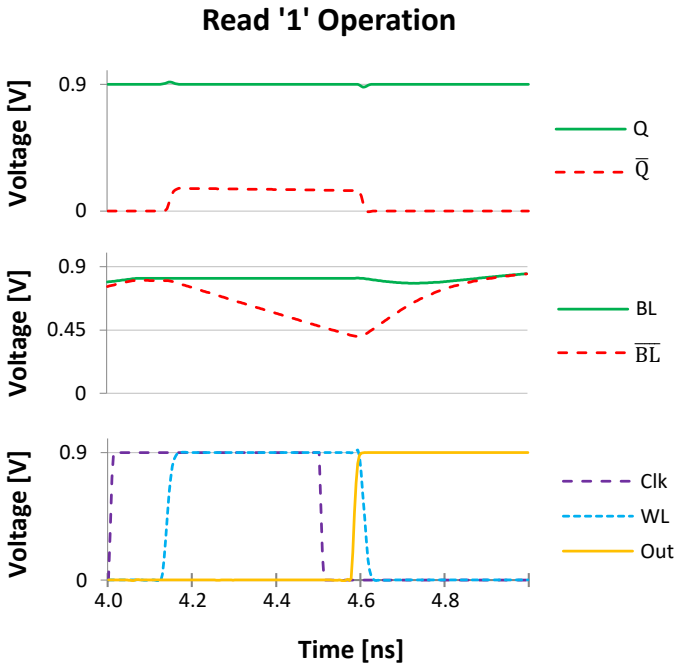


Figure 17: Simulation of a Read Operation on the designed memory cell.

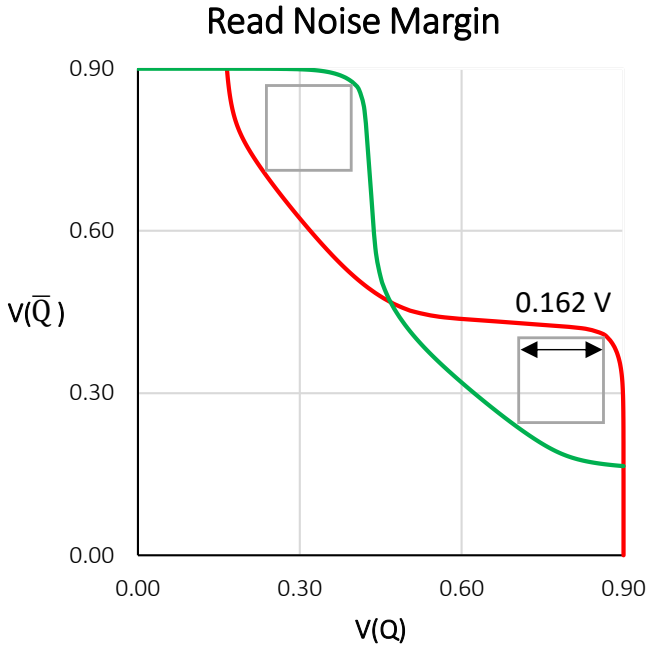


Figure 18: Read Noise Margin of the designed memory cell.

by the array and discharging one of the bit lines. In the same manner that SNM can be used to estimate stability during idle state, a DC analysis of the output of inverters can be performed to estimate the cell's stability during read operations. Larger values of Read Noise Margin (RNM) represent a better stability during read operations. This parameter can be improved by changing the number of fins on pull down, pull up and pass transistors of the cell. For the proposed cell designed with only one fin for each transistor, the RNM measured was 0.162 V. Fig. 18 depicts the butterfly plot of the RNM.

To evaluate the designed cell's power consumption throughout read operations, the current consumption of the cell's power supply was monitored. Fig. 19 depicts variation on the current when pass transistors are turned on by the activation of the word line. Power consumption was measured as the integral of the area illustrated in red and beige on Fig. 19 multiplied by the supply voltage, and divided by the period of the analysis. Thus, it was measured that power consumption during a Read Operation on the designed memory cell is $17.46\mu W$.

3.2.2 Write Operation

To perform a correct write operation, both BL and $\overline{BL}$ are driven with the values intended to be written. When word lines are activated, the bit lines overpower the cell with a new value. In the designed cell, write operations successfully write a new value on the cell in approximately 0.2 ns. A simulation example of this operation is shown on Fig. 20.

The power consumption of write operations was also evaluated. Likewise the

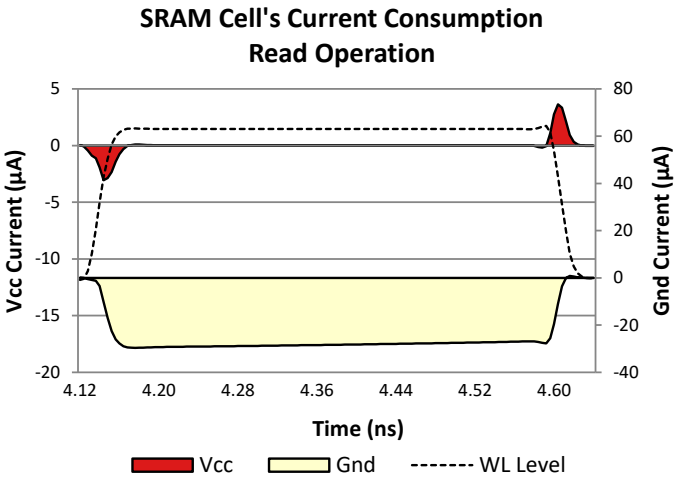


Figure 19: SRAM Cell's current consumption on Read Operations.

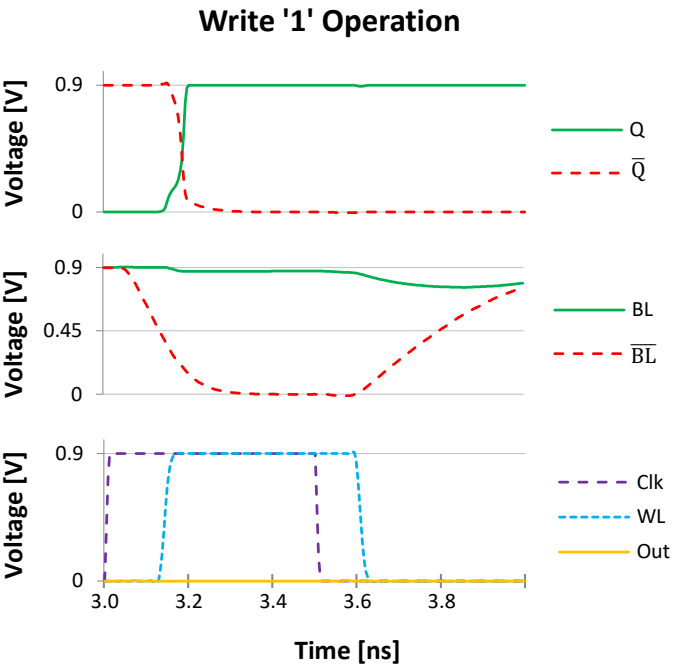


Figure 20: Simulation of a Write Operation on the designed memory cell.

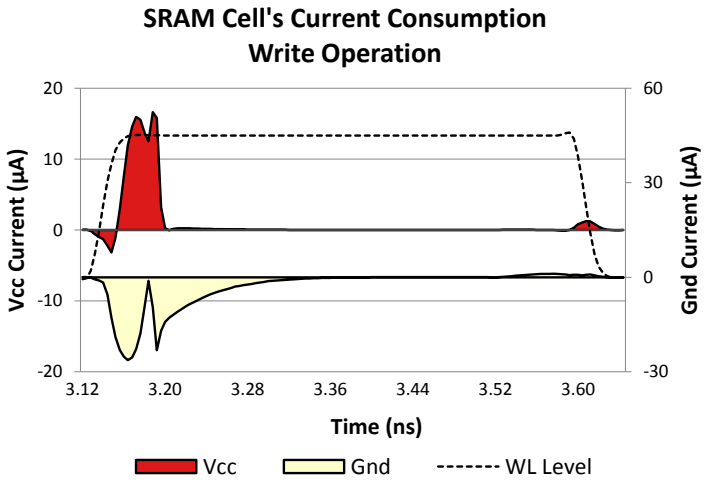


Figure 21: SRAM Cell's current consumption on write operations.

method used for read operations, power consumption was estimated using the integral of current consumption on the cell. Following the pattern for larger technologies, consumption on write operations was smaller than read operations, and was estimated on $8.5\mu W$

3.3 Peripherals

In order to evaluate the proposed methodology and analyze defects on FinFET technology, a small Static-Random Access Memory array consisted of FinFET-based 6T cell memories and peripheral devices was designed. To simulate an array of 1024 rows of 8-bit words, each selection line and signal were loaded with a capacitance load that had been previously measured. Each word line was charged with 203.2 fF, while bit lines were charged with 30.5 fF.

Three peripherals are used to ensure proper functioning. A precharger circuitry is used to pre-charge the bit lines to V_{DD} before operations. This circuit operates in opposition to the clock signal: when the clock signal is low, it activates the pre-charge circuitry. As soon as the clock signal is high, the precharger stops charging the bit lines. A signal named PC controls this circuitry. Fig. 22 depicts the schematic of the precharger adopted in this work.

To assist write operations, a write driver is used to enforce the new value on the cell. This circuit is controlled by the signal WE, and is activated whenever a write operation is performed. In this circuit, FinFET transistor are carefully dimensioned to assure the new value will be effectively written on the cell. The write driver's schematic is illustrated on Fig. 23.

The last peripheral on the array is a differential sense amplifier used to improve

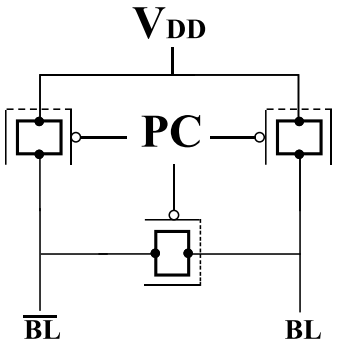


Figure 22: Precharger Circuit.

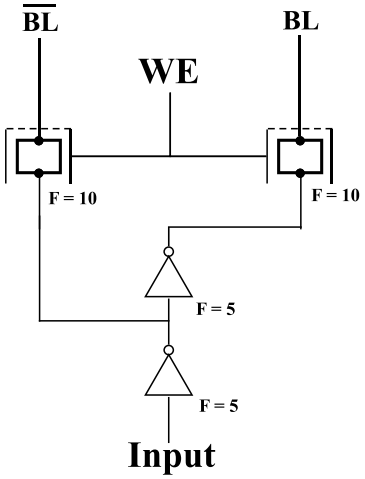


Figure 23: Write Driver Circuit.

read capabilities. The device reads BL and $\overline{BL}$ and estimates the ΔV between them. The result is then normalized to a strong logic value of '1' or '0'. This circuit is shown in Fig. 24.

3.4 Defect Modeling

In order to carry out an analysis on the impact of resistive defects on memory cells, electrical simulations have been performed on HSPICE simulator. A set of 12 defects were injected into memory cells, one at a time. Due to cell's symmetry, only one instance of each defect is necessary to analyze their impact on cell's behavior.

3.4.1 Resistive-Open Defects

From the set of twelve different defects injected, six of them are classic resistive-open defects previously studied for bulk CMOS technology (BORRI et al., 2005). In summary, resistive-open defects are non-designed resistances between two nodes that have a connection. Fig. 25 depicts the scheme adopted to model the resistive-open defects.

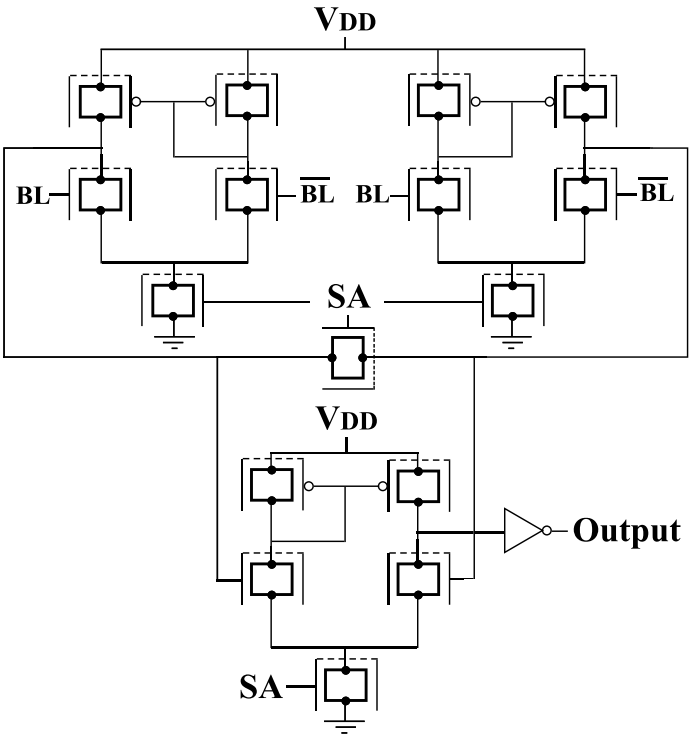


Figure 24: Differential Sense Amplifier Circuit.

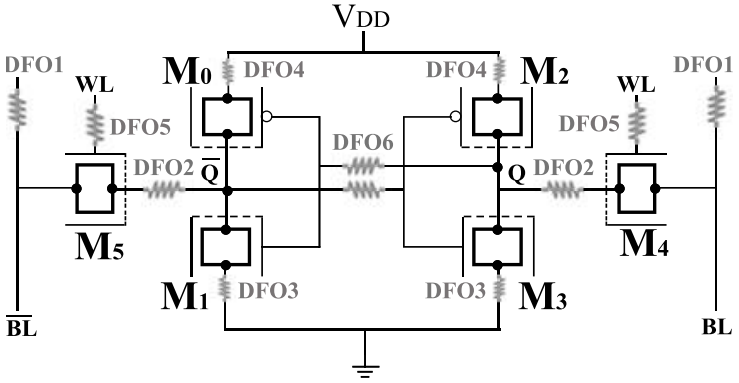


Figure 25: Resistive-Open defects injected in the proposed 6T FinFET-based SRAM Cell.

3.4.2 Resistive-Bridge Defects

The other six defects analyzed are considered resistive-bridge defects, which are resistive connections between nodes that, upon design, were not connected (DILILLO et al., 2005). Fig. 26 shows the set of resistive-bridge defects analyzed in this work. DFB1-DFB5 are classic resistive-bridge defects that have been previously analyzed in CMOS technology (FONSECA et al., 2010). To expand this analysis, another defect labeled DFB6 was modeled considering the resistive-bridge defect that can connect drain and source of transistors in FinFET technologies.

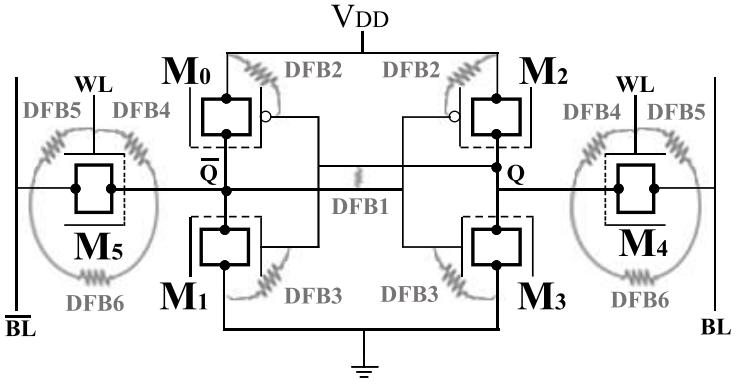


Figure 26: Resistive-Bridge defects injected in the proposed 6T FinFET-based SRAM Cell.

3.5 Specification of Hardware-Based Approach

For this work, the design of an On-Chip Sensor able to perform parametric analysis on circuit's signals in a way that eventual discrepancies observed during operations and caused by manufacturing defects could be identified was proposed.

In summary, the sensor should be able to monitor a signal – current consumption, voltage level – and generate a modulated response of this signal to such a degree that, when fed to a comparison logic circuitry, could be used to identify the existence of resistive defects.

This would take place during manufacturing test. After fabrication, memories would be subject to a parametric test aimed to identify discrepancies. By performing the same operation in the entire array, it is expected to observe the same behavior on monitored signals. However, if inconsistencies are observed between monitored signals, imperfect elements can then be flagged as defective and repair and replacing techniques can be used to swap or disable such elements and assure the reliability of the memory array.

Two sets of parameters were chosen to be monitored based on the analysis of simulations of the array when injecting defects. First, a more traditional approach that has been previously evaluated in planar technologies (LAVRATTI et al., 2015; LAVRATTI, 2012) that consists in monitor current consumption of both V_{DD} and GND of each column in the array using On-Chip Current Sensors. And secondly, the bit lines of each column were monitored and fed to the sensor with the intention to single out abnormal behavior. A diagram block demonstrating the overall application of the proposed hardware-based approach is presented on Fig. 27, where red OCCS represent the On-Chip Current Sensors responsible to generate modulated outputs based on one of the signals from the monitored pair of signals, while blue OCCS represent On-Chip Current Sensors responsible to generate modulated outputs based on the other monitored signal from the pair of signals;

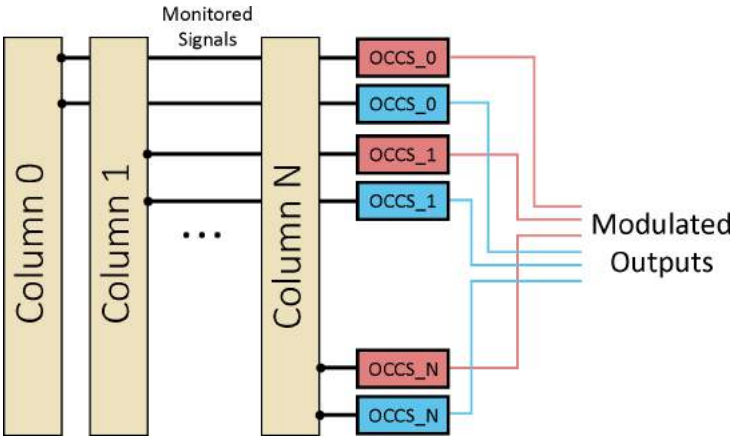


Figure 27: Architecture of the hardware-based approach.

for example, red sensors are responsible for V_{DD} while blue sensors are responsible for GND.

The designed sensor should be able to identify discrepancies in a wide range of defects size. As the main justification for this approach is that functional tests in FinFET-based SRAMs are not entirely reliable, this hardware-based methodology should be able to detect not only weak defects that do not sensitize any faults, but also weak defects that cause dynamic faults.

The On-Chip Sensor's design is not trivial. It is vital that all sensors present the same response, specially if these responses are used for comparison among themselves later. As any other circuit in the chip, the sensor is also subject to PV. This may have a severe impact on the output generated by the sensor and affect the methodology efficiency.

An additional challenge related to this hardware-based methodology is the noise aggregated to the monitored signals due to the presence of the sensor. By measuring the voltage level or current consumption, sensors aggregate a resistance in series to the measured signal, thus creating a disturbance in the monitored node's voltage. The hardware-based approach proposed in this thesis is based on the insertion of On-Chip Sensors that will monitor the cell's behavior in order to identify the presence of defects. The sensor should aggregate the least possible noise disturbance in the circuit. To achieve this, operational amplifiers are ought to be used to amplify the monitored signal so it can be manipulated by the following stages.

Other important design aspect of the sensor is the overhead in area and power. Considering that this test methodology would be used alongside other recovering methodologies, it is desired a minimal impact on circuit area and power consumption. As there are no physical layouts for the FinFET technology model adopted, area overhead was measured as the relation between the number of fins of transistors in a monitored circuit (i.e. a memory column) and the number of fins of transistors present in the hardware-based

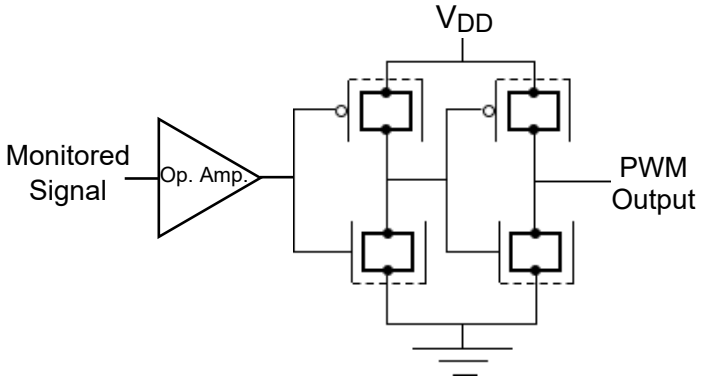


Figure 28: Diagram of both stages of the designed sensor.

methodology. This way, it is possible to estimate area overhead's percentage. For power overhead, a simple current consumption comparison, before and after the methodology's introduction on the memory array, was carried out.

3.6 Implementation

The sensor designed for this work is based on other sensors and other similar approaches in literature. Specifically, the sensor in this work was designed following a similar methodology proposed in (LAVRATTI, 2012). As current consumption in FinFET technology is smaller than in planar technologies, the operational amplifier has to be well dimensioned to correctly amplify the monitored signal. This way, the dimensioning of transistors followed recommendations from similar works and text books (SEDRA; SMITH, 2010).

The sensor was implemented in two distinct blocks, regardless of the signal monitored. First, the monitored signal is subjected to a two-phase operational amplifier that generates pulses whenever the monitored signal is not on its normal state (i.e. nominal voltage, ground voltage). This pulse is then modulated in a digital Pulse Width Modulation (PWM) circuit. The scaling of each circuit is highly dependent on the monitored signal. Fig. 28 depicts both stages of the sensor.

The two-stage operational amplifier operates in two steps. Schematics with corresponding denominations of transistors can be seen in Fig. 30 and Fig. 31. First, reference signals are generated. The signal to be used in the differential pair as a reference to be compared with the monitored signal is generated by MR1, MR2, and MR3, while the reference current is generated by the current generator. The current mirror generated by M8 and M5 supplies to the differential pair M1 and M2 the bias current. The input differential pair is actively load with the current mirror generated by M3 and M4. The second stage is composed by M6, which is a common-source amplifier loaded with the current-source M7. A capacitor C_C is included in the negative-feedback path of the second stage and is

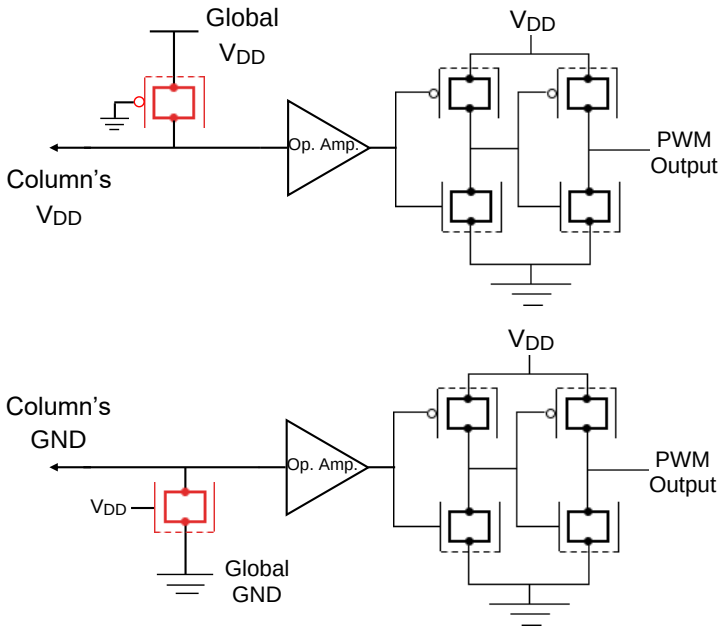


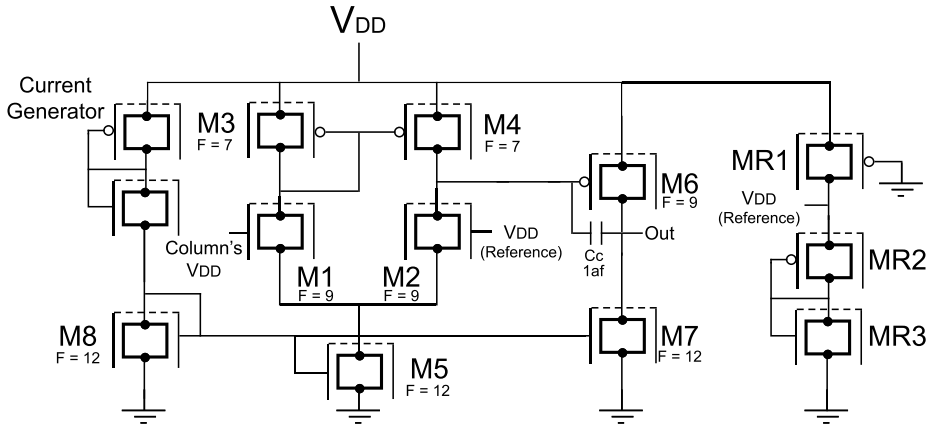
Figure 29: Diagram of the designed sensor for the current consumption monitoring approach.

intended to enrich the Miller effect, which has a direct impact on the frequency response of amplifiers. However, the frequency response analysis of this amplifier is not within the scope of this work.

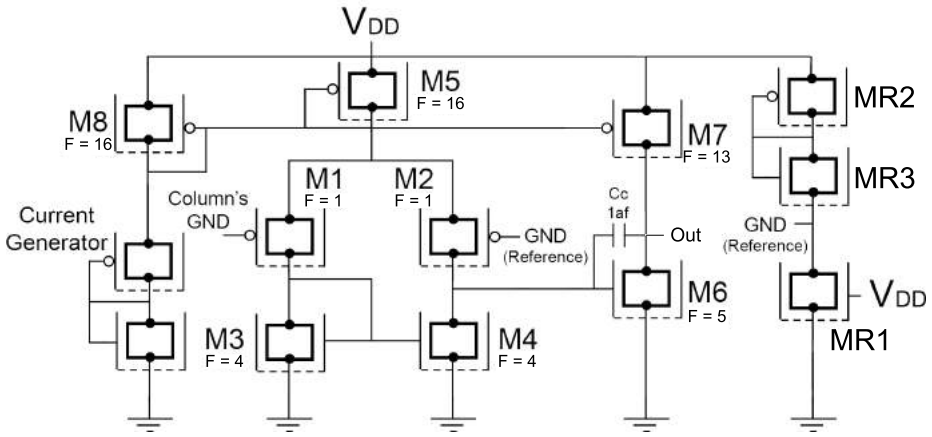
3.6.1 Approach 1: Current Consumption

Previous methodologies have studied this approach to identify discrepancies caused by resistive-open defects in memory arrays (LAVRATTI et al., 2015; LAVRATTI, 2012). In this approach, each column in the array has its own voltage source. This strategy allows monitoring the consumption of V_{DD} and GND in each column. During the execution of operations, the sensor monitors the current consumption on the designed cell, plus the leakage consumption on all other cells of the column. However, as show in section 3.2, the sum of all leakage current from all other cells in a column is irrelevant when considering the consumption of a write or read operation.

As the sensor is monitoring both V_{DD} and GND, it was necessary to design the sensor with specific dimensions for each signal. Additionally, a current to voltage converter is also inserted prior to the operational amplifier. This low amplitude voltage signal is used as power supply / ground by the column and monitored by the sensor to generate its output. The schematic of both models of sensors designed for this approach is illustrated in Fig. 30, while Fig. 29 shows the diagram of the sensor including the converter.



(a) V_{DD} Sensor.



(b) GND Sensor.

Figure 30: Schematic of the designed current consumption sensor.

3.6.2 Approach 2: Bit Line Voltage Level

As previously mentioned, bit lines were also monitored to detect abnormal behaviors. The same two-phase operational amplifier followed by a PWM circuitry was adopted for this approach, only with different dimensions. However, the use of a current to voltage converter became unnecessary. Fig. 31 depicts the schematic of the designed sensor for this approach.

3.7 Detection Logic

To estimate the efficiency of the sensor proposed, a detection logic based on neighborhood comparison previously evaluated on (LAVRATTI, 2012) was aggregated to the circuit. The detection logic is composed of logic gates that compare the results gathered by the sensor and compare them in groups of 4 signals. The detection structure and it's efficiency in CMOS applications were thoroughly studied on (LAVRATTI, 2012), so these topics will not be covered in this work. Nevertheless, it may be interesting to analyze the viability of this detection logic structure when considering applications using FinFET

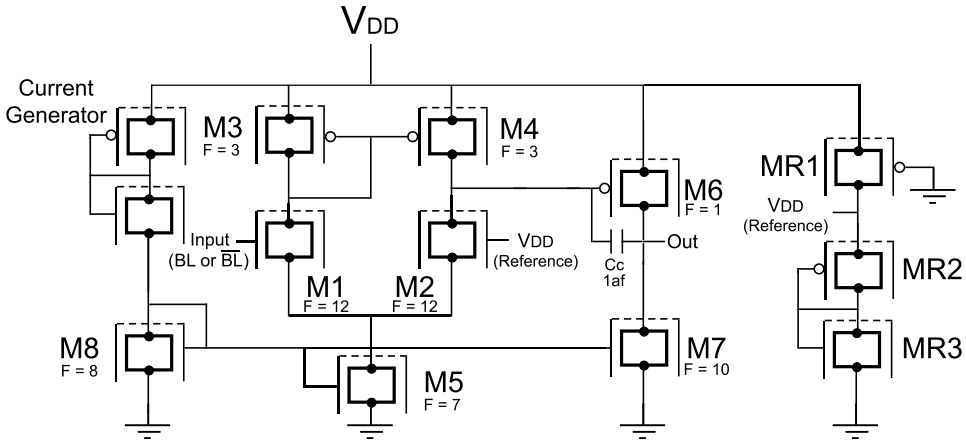


Figure 31: Schematic of the designed voltage level sensor.

technology.

This circuit considers a group of 4 signals to identify the presence of resistive defects, and analyzes neighbors signals by comparing immediate neighbor signals. Thus, in a group containing four signals, each one is compared with other two signals. If no discrepancy was detected in the analysis of one signal, then the same behavior was observed in the majority of signals in that group - which absents the analyzed signal plus its two immediate neighbors from defects. All four signals are subjected to this analysis, which provides a full diagnosis on all signals.

Even though this detection logic is able to provide the localization of resistive defects (or at least the presence of one or more defects), its application in FinFET memories may not be feasible. As previously stated, this detection logic considers a column as fault-free only when its behavior matches other two neighbor columns. This may be difficult to observe in FinFET technology due to process variations. Hence, different detection logic methodologies, specially ones that require smaller set of signals for analysis, represent a better option for the detection of resistive defects on FinFET memories through parametric testing.

4 Validation

With the proposed approach and its requirements specified and implemented, a validation step was carried out to assure the proper functioning of the memory array, its peripherals, and the proposed sensor.

Validation was performed in three steps. First, the implemented memory array and its peripherals were validating considering its functionality. In a second moment, resistive defects were injected, one at a time, in memory cells to measure the impact of each defect. A comprehensive behavior characterization was carried out, and an interval of fault-free operation was defined. Once the impact of all resistive defects injected were fully explored, each approach of the proposed methodology was aggregated to the array to validate its functionality. All three steps were performed on a nominal temperature of operation of 27°C. Analysis considering other temperatures are investigated during the evaluation step described on Chapter 5.

4.1 Experimental Setup

The SRAM array adopted during simulations is composed of 8 rows of 8 cells each. However, bit lines and word lines are charged with capacitive loads relative to an array of 1024 rows by 128 cells, emulating a 16k Bytes memory array.

The SRAM block has 4 inputs, and 1 output. A clock signal with frequency of 1 GHz synchronizes the array and peripherals, and is used to generate other control signals as well. A single-bit control signal indicating the operation mode (read / write) is also fed to the block. A 3 bit signal indicates the address of operation, while an eight bit signal is used as input for the data about to be written. Another eight bit signal is used to output the data read from the cells.

Each column of the array has a set of the peripherals defined in section 3.3. In summary, a write driver, a differential sense amplifier, and a precharger are responsible for the proper functioning of the column. A 3-to-8 decoder is also used to select the correct row of operation. The organization of the circuit just described is shown in Fig. 32.

4.2 Fault Mapping on FinFET SRAMs

To identify logic faults on FinFET SRAM cells affected by manufacturing defects, it was carried out an extensive mapping process using an automated tool developed for this work. This tool aimed to simulate the memory block with the designated group of

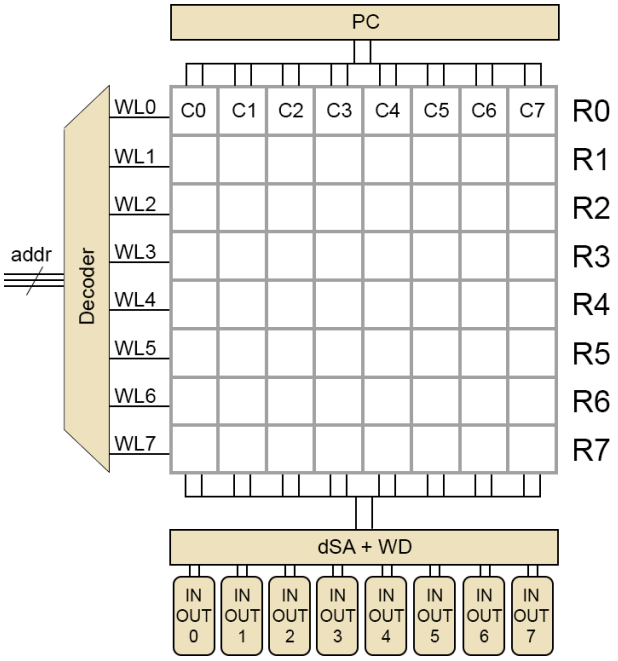


Figure 32: Organization of the SRAM Memory array and its peripherals.

defects and trace faulty behaviors by monitoring output signals and internal states of cells. This procedure was divided into two parts: first, the tool simulated the circuit with progressively bigger defects sizes until an inconsistent behavior was detected; the tool would simulate the same defect, but slightly smaller than during the previous iteration. It is important to emphasize that "stronger defect" has a different meaning for opens and bridges defects. For resistive-open defects, a stronger defect is one with greater resistance. For resistive-bridge defects, the opposite applies, and stronger defects have smaller resistance. These iterations persisted until a critical resistance, which is defined as the threshold between expected behavior and faulty behavior, was defined for each defect and fault model observed in the defect as well.

To validate the results obtained through the tool and correctly categorize the faults observed, waveforms generated on HSPICE were visually analyzed. At the end of the entire process, the set of data was assembled to define intervals of fault-free operation. The results obtained on Resistive Open defects are shown on Fig. 33, while Fig. 37 shows the results for Resistive Bridge defects. An example of the tool's report is shown in Annex B.

4.2.1 Resistive-Open Defects

This section briefly summarizes the results obtained through the process of mapping faults caused by resistive-open defects injected into the memory array, and then investigate some of the most notable behaviors observed. Defects injected varied from a range of 1Ω to a maximum of 30MΩ. Fig. 33 shows the critical resistance of each defect.

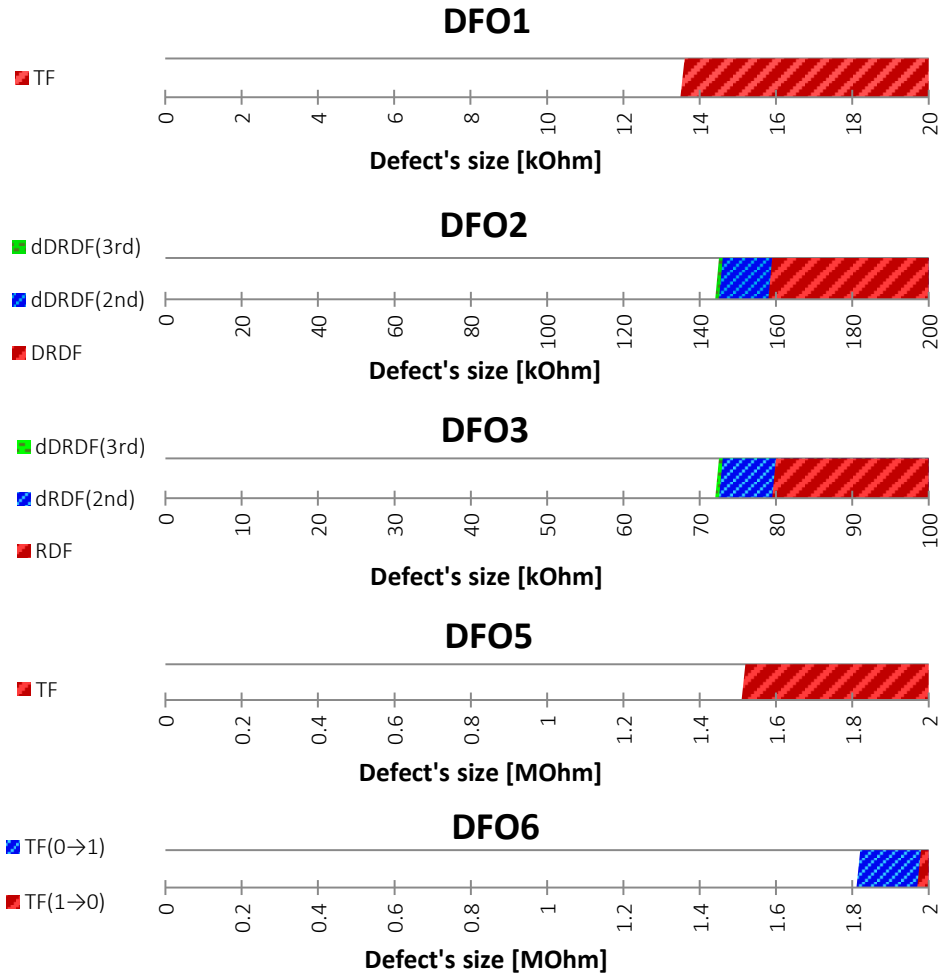


Figure 33: Faults observed on cells affected by Resistive Open defects.

It is interesting to note that DFO4 does not sensitize any faults in nominal temperature, which follows observations from other similar works (LAVRATTI, 2012).

It is important to note that some of the dynamic faults that will be explored momentarily, for both resistive-open and resistive-defects, are not show in Fig. 33 and Fig. 37. This is due to the step in which the figures showing the results from the mapping process were arranged. For example, for a certain defect, faults observed were arranged in a step of 500Ω. At a resistance of 50kΩ, no fault was observed. The next step in the figure would be 50.5kΩ, where a dynamic fault was observed after two operations. Thus, faults in between these two values are not shown in the diagram.

Overall, the faults observed on cells affected by resistive-open defects can be summarized as Transition Faults and Destructive Faults. Fig. 34 illustrates the first case. It shows a cell affected by a resistive-open defect that creates a discrepancy in the bit lines (DFO1). A write '1' ($w1$) operation is unsuccessfully executed on the cell. As BL cannot overpower the new value in the cell, the transition on the cell fails.

Fig. 35 and Fig. 36 illustrate the occurrence of dynamic faults on cells affected

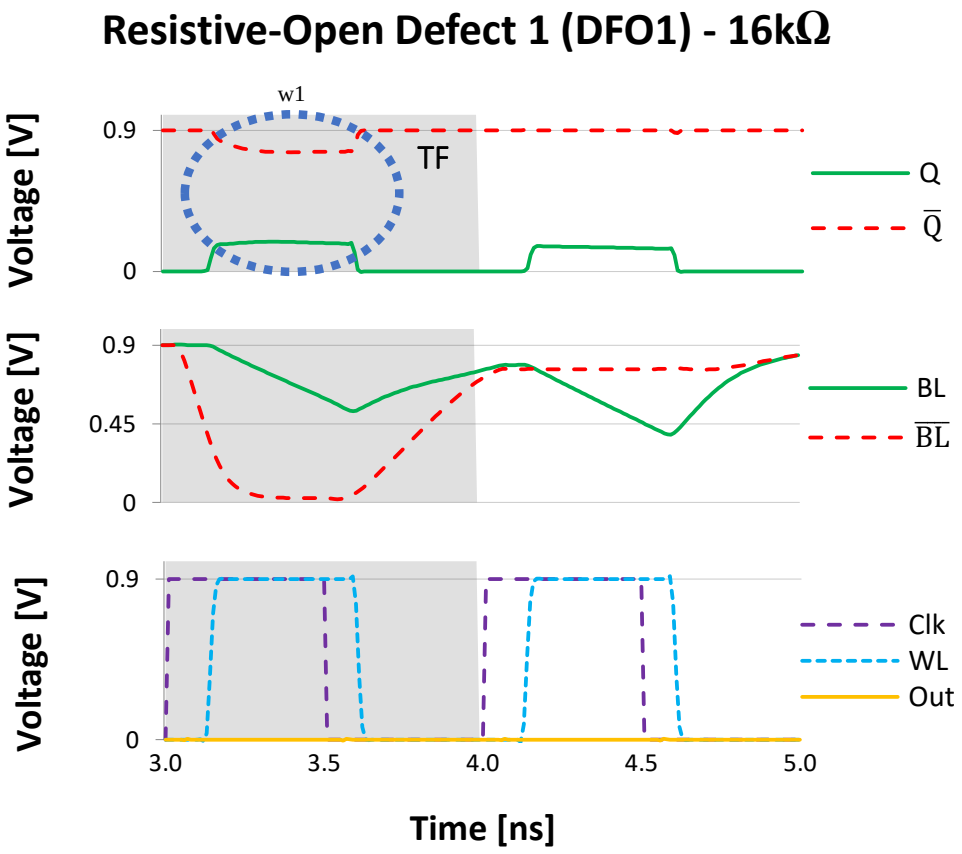


Figure 34: A TF on a cell affected by a DFO1 of 16kΩ.

by resistive-open defects. First, it is shown the simulation of a memory cell affected by a resistive-open defect that creates a discrepancy in the connection between pass-transistors and nodes Q or $\overline{Q}$ (DFO2). A successful write '0' ($w0$) is followed by consecutive read operations. As can be observed by the bit lines, the defect prevents the discharge of BL. On the third consecutive read operation, the value stored on the cell flips. As the new value on the cell is not outputted by the read operation, this fault observed is categorized as a dDRDF (3^{rd}).

The second case of dynamic faults caused by a resistive-open defect is shown next. The simulation of a cell affected by a resistive-open defect that creates a discrepancy in the connection between the pull-down of inverters and GND (DFO3) is illustrated in Fig. 36. A $w1$ operation writes the value '1' on the cell, and is followed by consecutive read operations. Even though the operations appear to be executed correctly (at least functionally, as the sense amplifier is able to generate the correct output), the bit lines indicate that the cell is not able to correctly discharge $\overline{BL}$ during read operations. After six consecutive operations, the seventh read operation performed on the cell flips the value stored on the cell, and this new value is only outputted on the following read operation. Thus, this fault is defined as a dDRDF (7^{th})

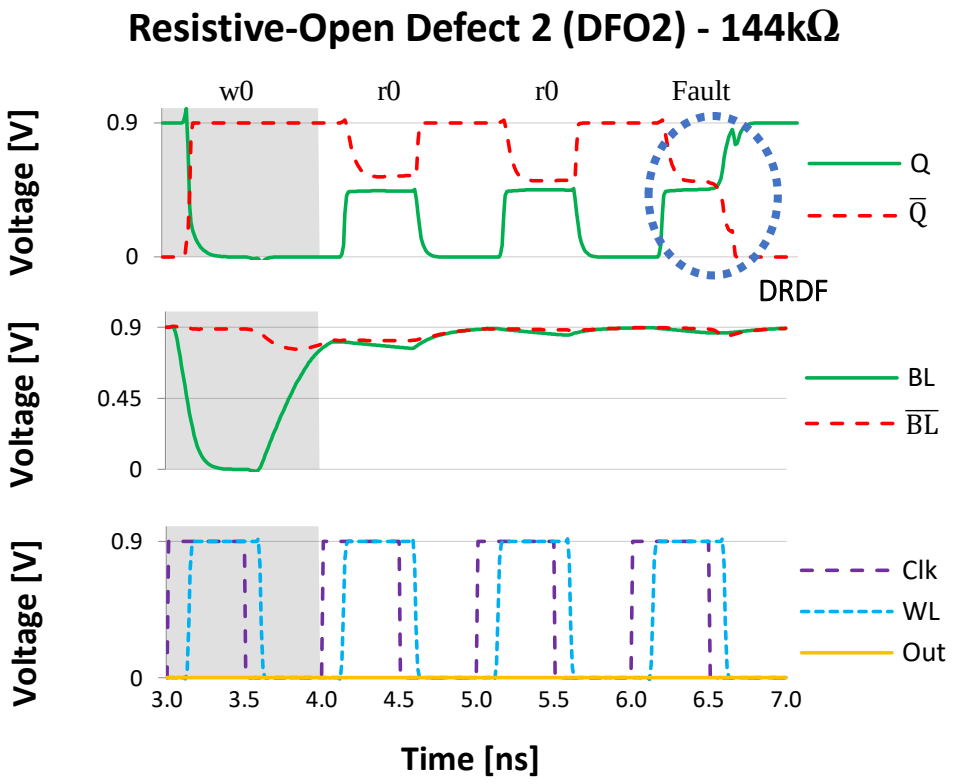


Figure 35: A dDRDF on a cell affected by a DFO2 of 144kΩ.

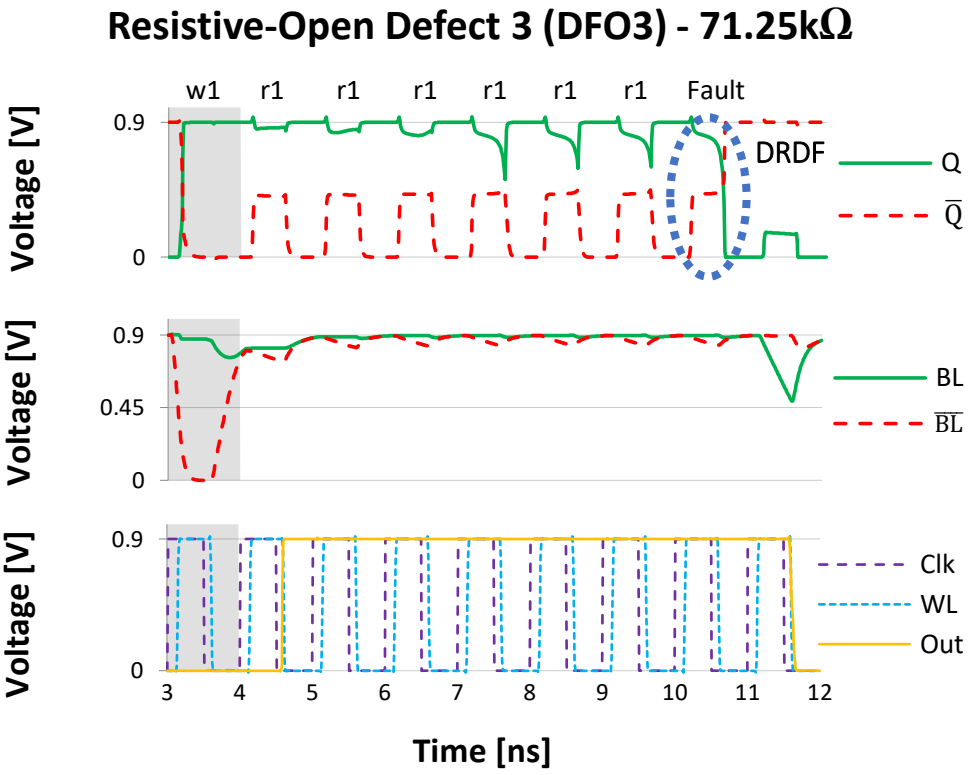


Figure 36: A dDRDF on a cell affected by a DFO3 of 71.25kΩ.

4.2.2 Resistive-Bridge Defects

Likewise the previous section, this section briefly summarizes and explores some of the results obtained in the fault mapping process for resistive-bridge defects. The process of finding faults on cells affected by resistive-bridge is more complex than for resistive-opens due to the possibility of connection between the cell and signals from the block (e.g. Word Line, Bit Lines). Thus, one should also verify the existence of linked faults (e.g. CFds) or isolated faults in other cells when analyzing the impact of this type of defect. Fig. 37 shows the critical resistance of each fault model observed during simulations. The results shown in the array impact are specifically interesting as their critical resistance is at least double the magnitude when compared to the cell itself, meaning that resistive-bridge defects that can affect the entire column may be more threatening to other cells than to the defective cell.

The set of faults observed in cells affected by resistive-bridge defects includes other faults that were not observed resistive-open defects. One of these faults is presented in Fig. 38, which shows a cell affected by a resistive-bridge defect that creates a connection between Q and $\overline{Q}$ (DFB1). If not very strong, this defect prevents these nodes to stay at V_{DD} or GND. It also affects the reliability of read operations, as can be observed by the voltage level on Q, $\overline{Q}$, BL, and $\overline{BL}$. While write operations are performed correctly, read operations cause the value in the cell to shift to $V_{DD}/2$. The Sense Amplifier fails to output the correct value due to the small ΔV between bit line. This behavior is classified as a WRF. It is interesting to observe that following read operations are able to output the correct data. This is due to the small recovery that happens in bit line's voltage between read operations.

If this same defect is stronger, a different fault is observed. Instead of jeopardizing the nodes' stability to stay in V_{DD} or GND, the defect forces both Q and $\overline{Q}$ to $V_{DD}/2$, characterizing an NSF. Read operations also fail to output the correct data, and the recovering behavior observed before is not present in this case.

Dynamic behaviors are also present in cells affected by resistive-bridge defects. Fig. 40 shows the simulation of a cell affected by a defect that creates a connection between nodes Q or $\overline{Q}$ to GND (DFB3). After a successful $w1$ operation, thirteen consecutive read operations were necessary to sensitize a fault. The observed fault was categorized as a dDRDF (13^{th}) as the read operation failed to output the new, yet incorrect value. More than just showcasing the existence of dynamic behavior in FinFET technologies, this also proves the necessity of other methodologies that do not rely on consecutive operations for diagnosis, since the number of demanded Read Operations varies according to defect size.

There is a different aspect of resistive-bridge defects that brings special attention

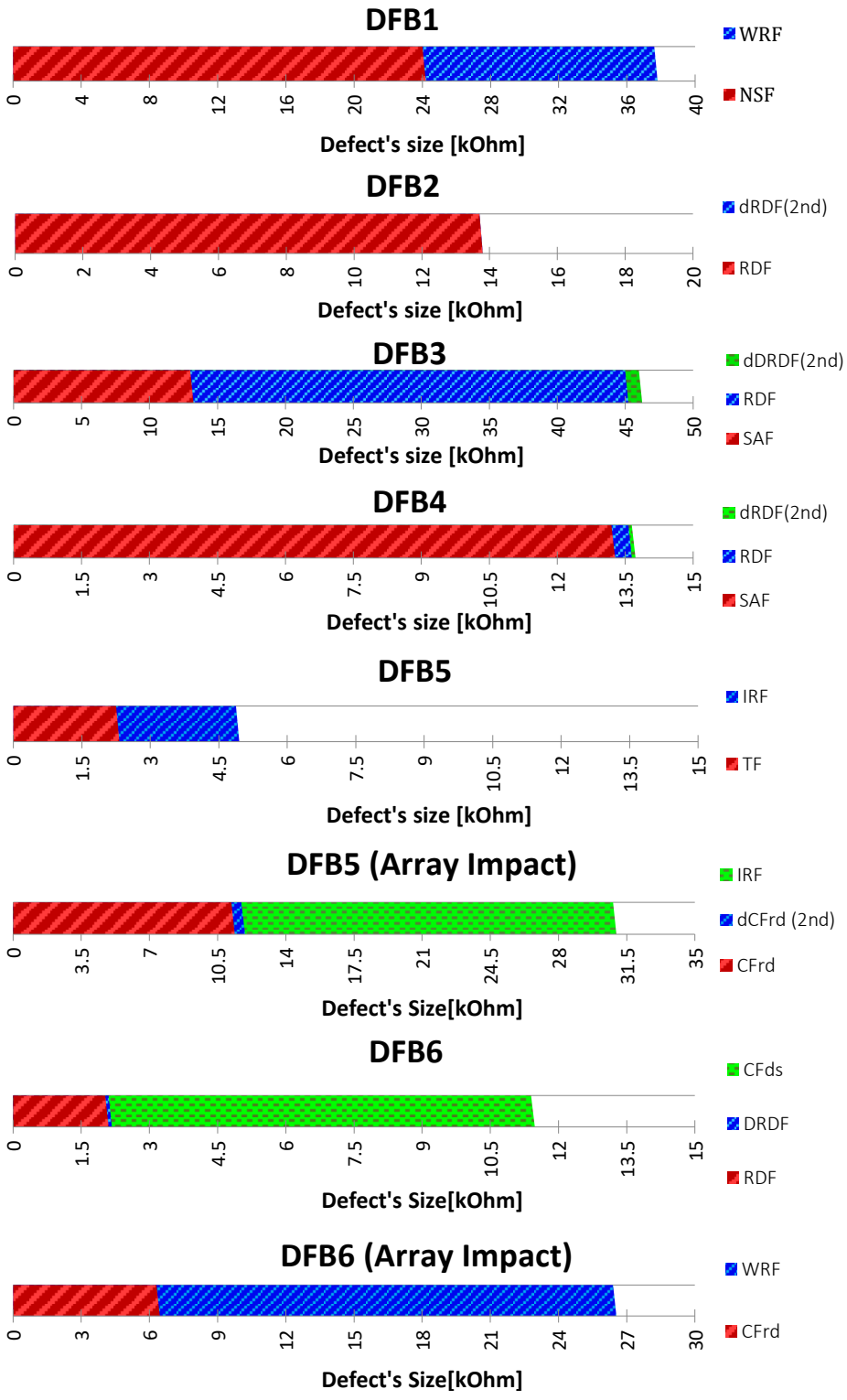


Figure 37: Faults observed on cells affected by Resistive Bridge defects.

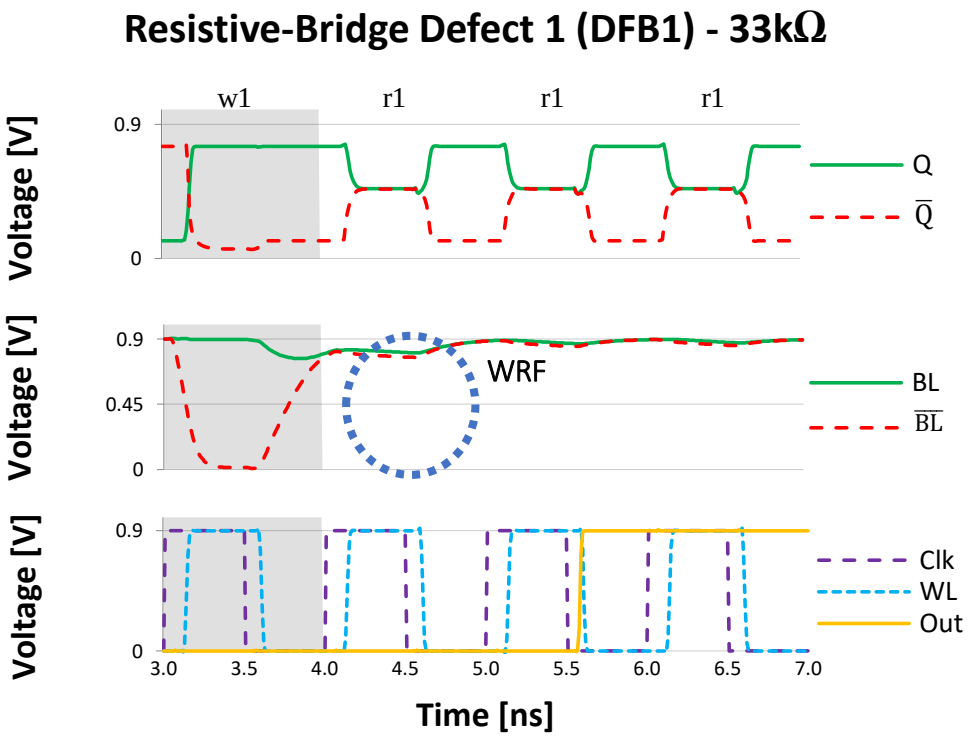


Figure 38: A WRF on a cell affected by a DFB1 of 33kΩ.

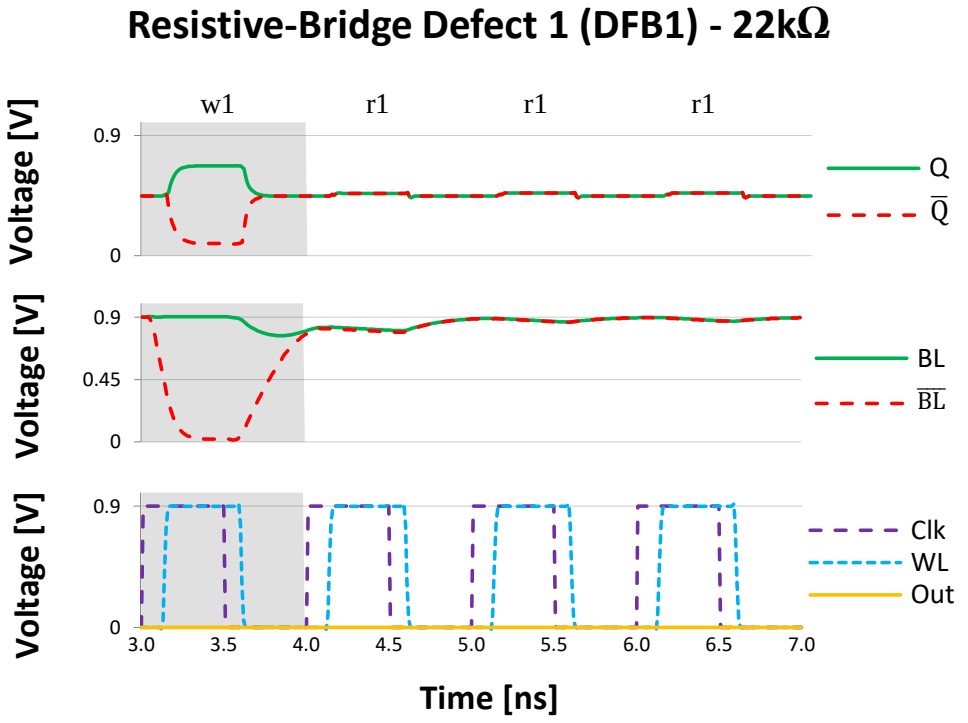


Figure 39: A NSF on a cell affected by a DFB1 of 22kΩ.

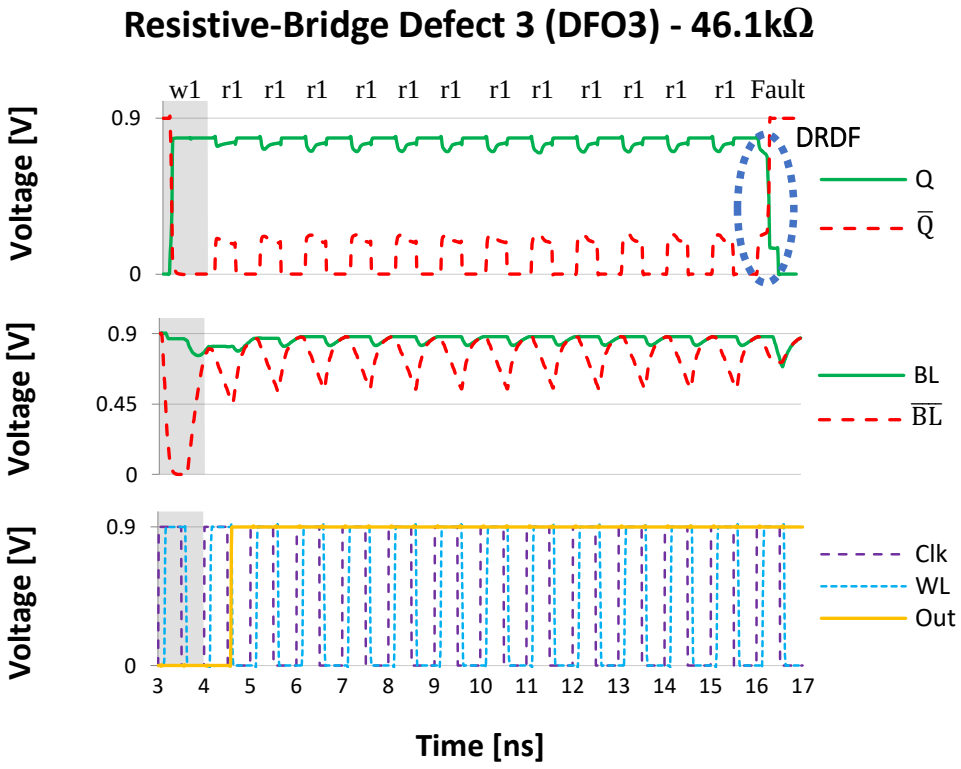


Figure 40: A dDRDF on a cell affected by a DFB3 of 46.1kΩ.

to the results. As they create connections, a resistive-bridge defect affecting one cell may impact other defect-free neighbor cells. Observing Fig. 41, it is possible to see the simulation of a cell located at row 0 and affected by a DFB5, which creates a connection between the word line 0 (WL0) and $\overline{BL}$ of magnitude 11.5kΩ. This defect size does not sensitize any fault in the observed cell, as was shown in Fig. 37. A write '0' operation is successfully performed on the cell, followed by three successful, consecutive read operations in the same cell on row 0. This defect starts to pose a reliability issue as operations in different rows are performed.

By performing a read operation on row 1, $\overline{BL}$ is not able to charge as it is being drained by WL0. This results in an IRF, as can be seen by the Out signal. As all three of the analyzed cells presented in Fig. 41 are located on the same column, they all share the same output signal. A subsequent read operation has a bigger impact, causing a dynamic CFrd on the cell. The same destructive behavior is observed when realizing subsequently read operations in another fault free cell located on row 2 but within the same column, this time a static CFrd.

More than that, operations performed on fault-free cells can affect defective cells as long as they are in the same column. Fig. 42 illustrates this fault behavior on a cell affected by DBF6 of magnitude 10kΩ, which created a resistive-bridge between source and drain of transistor M5, connecting $\overline{BL}$ and $\overline{Q}$. In Fig. 37, this behavior is classified as a Read Disturb Coupling Fault (CFds). As the fault-free cell on row 2 is written, the value

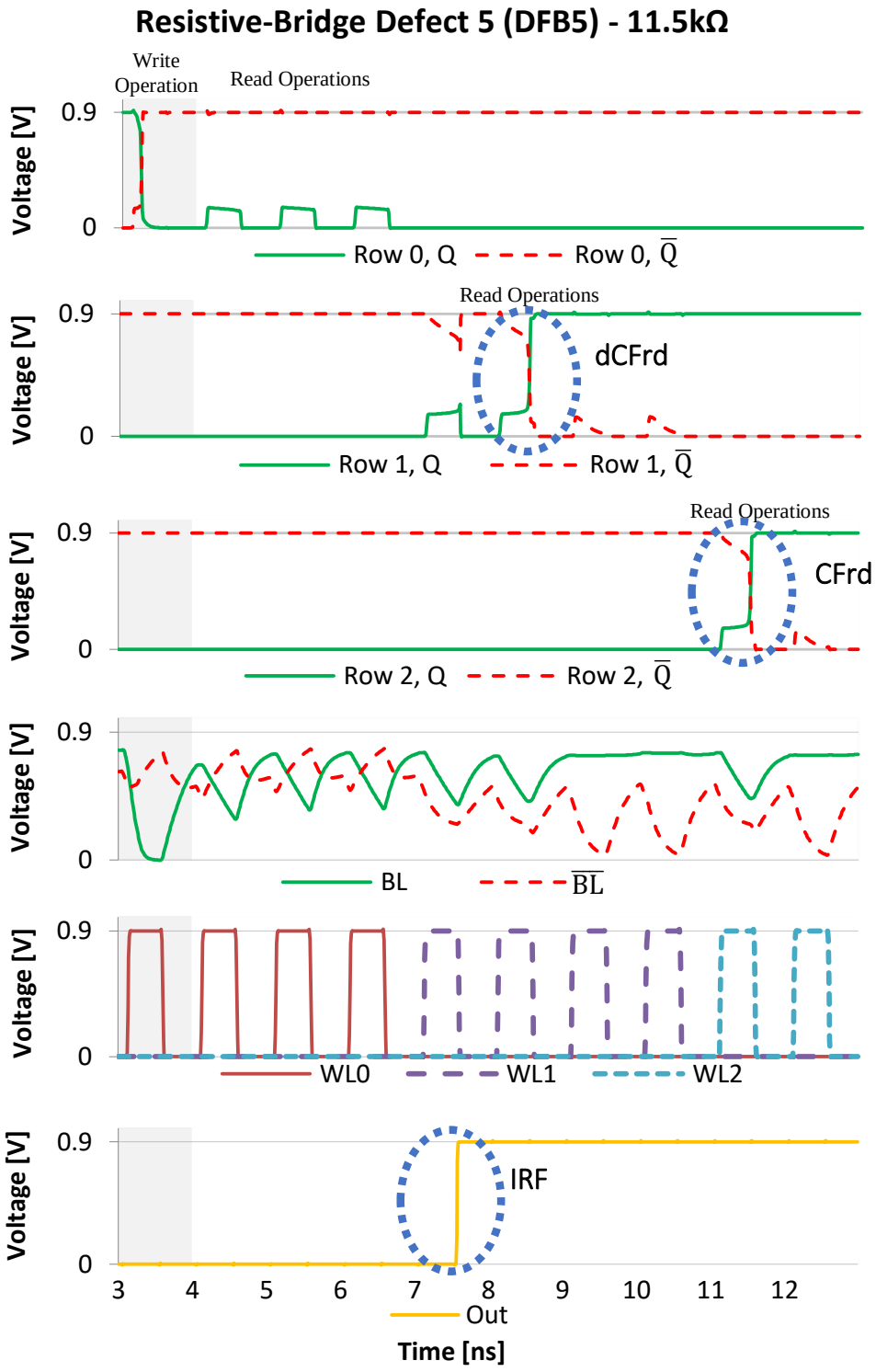


Figure 41: Faults observed in the column of a cell affected by a DFB5 of 11.5kΩ.

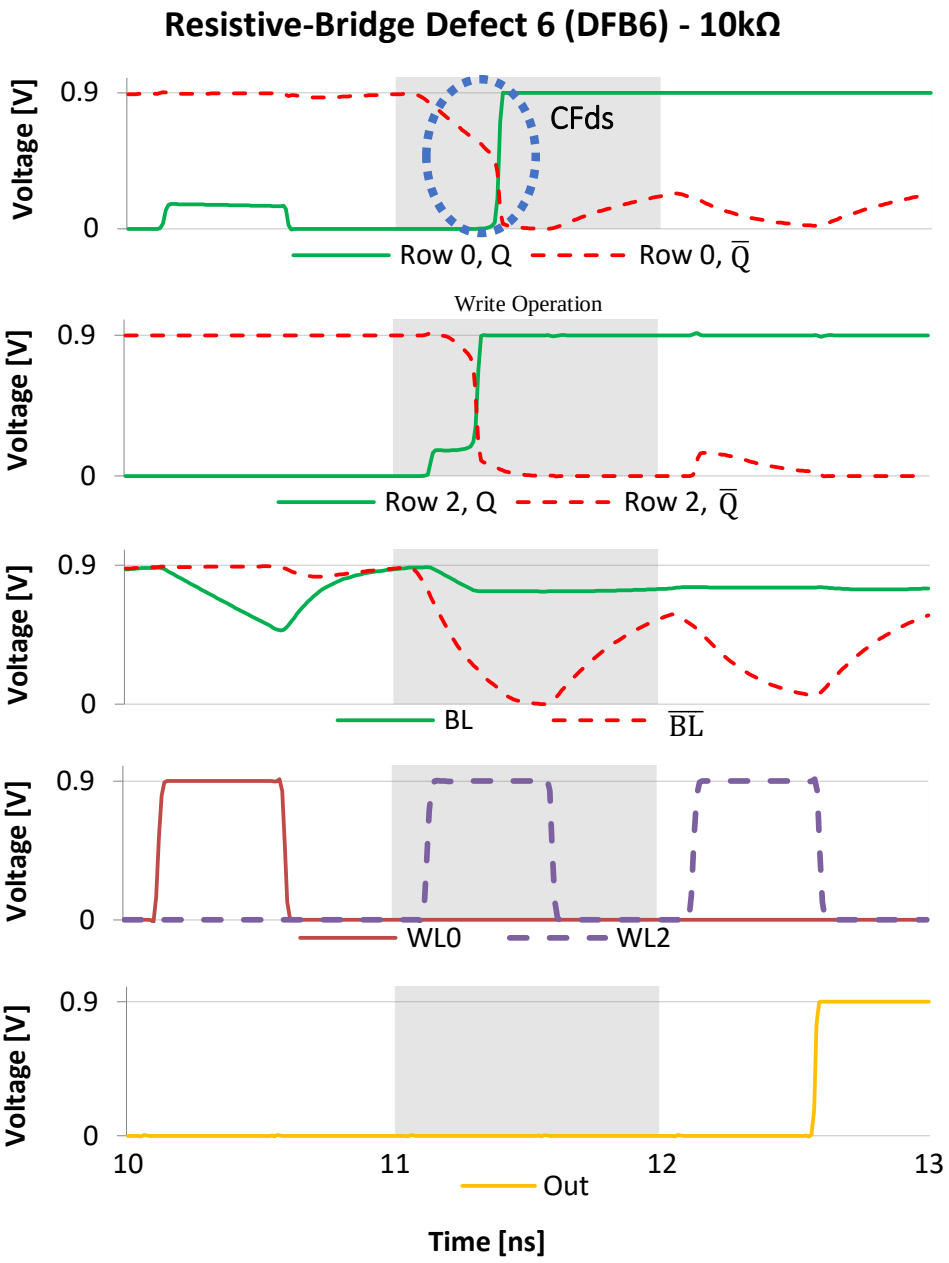


Figure 42: Simulation output of a cell affected by a DFB6 of 10kΩ suffering a CFds fault caused by an operation in a neighbor cell.

on the defective cell on row 1 cell is flipped. This happens due to the shared connection between $\overline{BL}$ and $\overline{Q}$. As $\overline{BL}$ is discharged owning to the write '0' operation, $\overline{Q}$ discharges as well, causing a misbalance, and eventually a flip on the stored value. This can also be considered as a "following-signal" behavior, as $\overline{Q}$ follows the value on $\overline{BL}$. This same behavior can be observed on cells affected by DFB4, as the affected node is now connected to the word line.

Fig. 43 depicts this particular behavior. It shows the simulation of a cell affected by a DFB4 of magnitude 13kΩ. In Fig. 37, this behavior is classified as SAF. This defect creates a connection between $\overline{Q}$ and WL. First, is it possible to observe a successful tran-

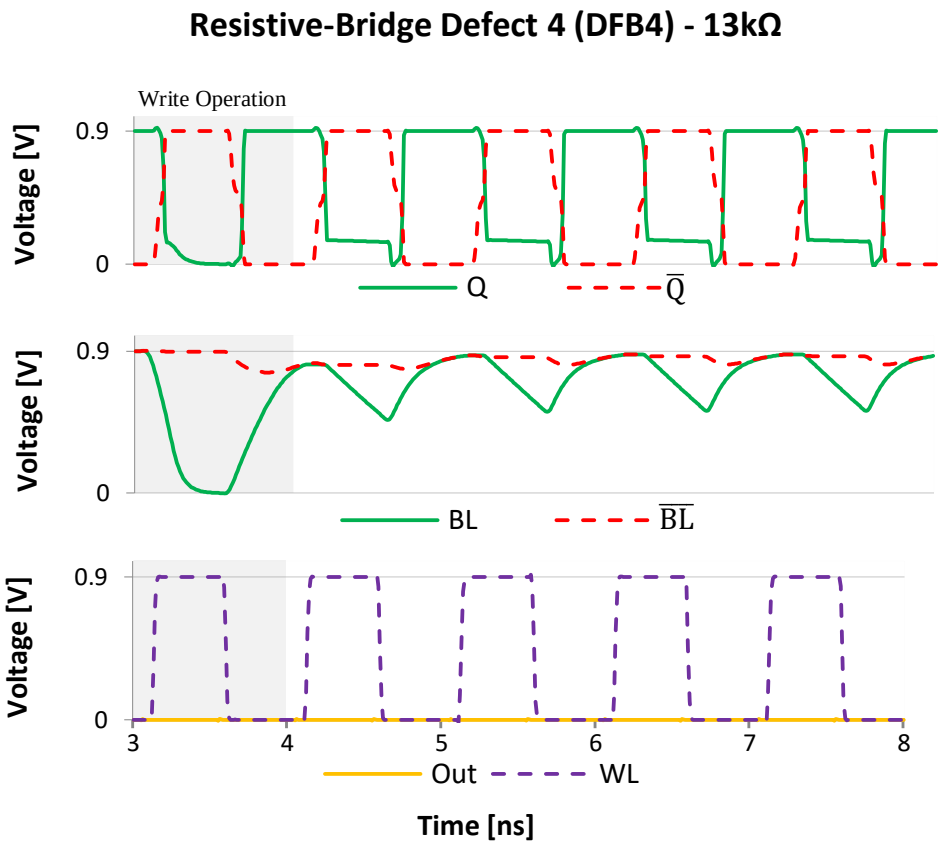


Figure 43: Simulation output of a cell affected by a DFB4 of 13kΩ.

sition from '1' to '0' caused by a $w0$ operation. However, as the word line is deactivated, the voltage on node $\overline{Q}$ drops immediately, causing a flip on the value stored. The cell keeps retaining the value '1' until the word line is activated again, when it momentarily stores and also outputs the value '0'. This way, $\overline{Q}$ follows the voltage on WL, causing an inconsistent behavior that may not be trivial to detect. The behavior observed resembles an SAF as the cell can only store '1' while the word line is off.

4.3 Validation of the proposed methodology

As stated previously, the methodology was divided based on two different monitoring strategies: (1) monitoring the current consumption in each column, and (2) monitoring the voltage level of both BL and $\overline{BL}$ in each column.

To validate both approaches, the SRAM block presented in Section 4.1 consisting of 8 rows by 8 columns (but loaded with a capacitance to emulate a 1024 x 128 array) was used. A march test executing an algorithm that access each cell five times and described in Algorithm 2 with a frequency of 1 GHz was adopted. All simulations were performed using the HSPICE simulator (v. J-2014.09-1) set to an operation temperature of 27°C.

Algorithm 2 March Test Adopted

$\Downarrow (w1)$;
$rst\_detection$;
$\Downarrow (w0, r0, w1, r1)$;

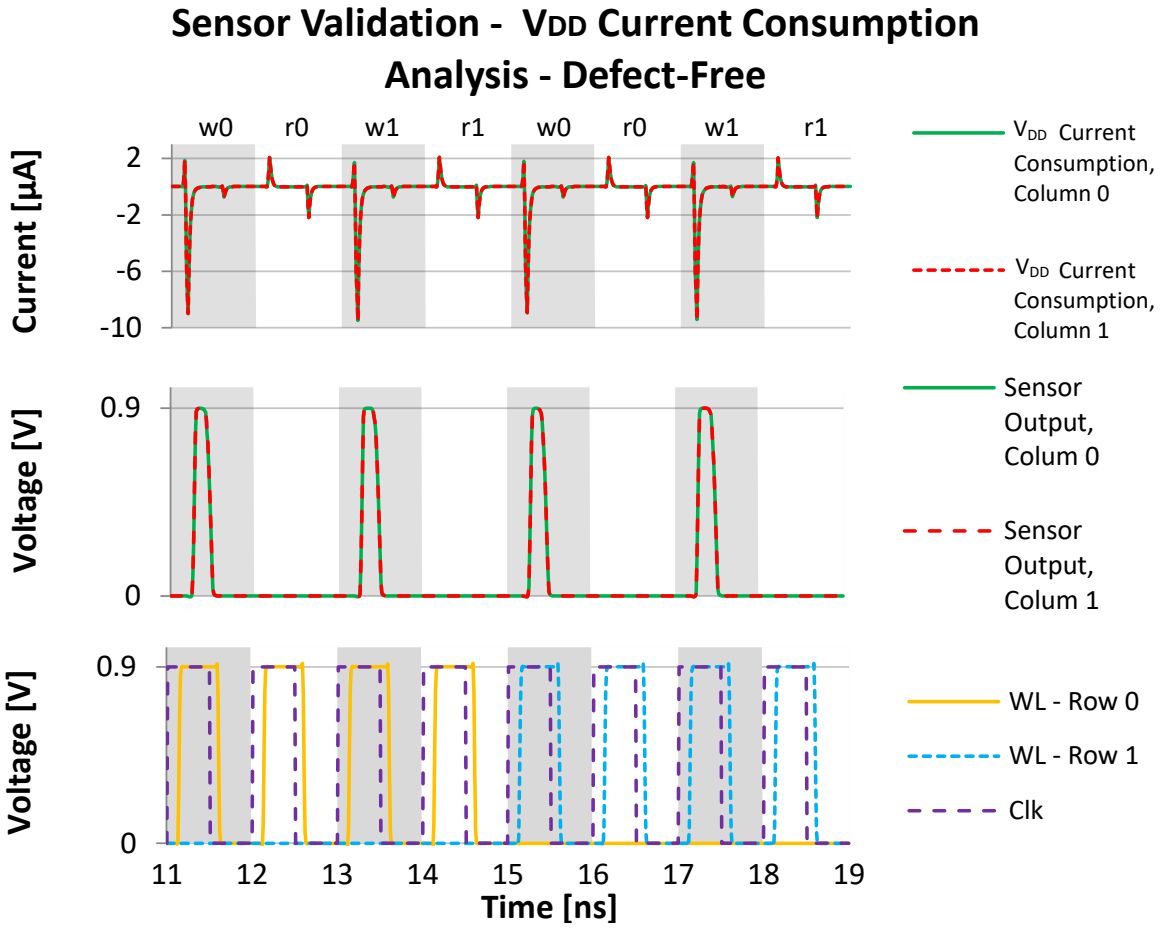


Figure 44: Sensor output when monitoring V_{DD} current consumption on defect-free columns.

4.3.1 Approach 1: Current Consumption

To validate the proposed strategy based on the monitoring of current consumption, both V_{DD} and GND consumption were monitored. Fig. 44 presents the simulation of the V_{DD} Sensor while monitoring two distinct columns that have not been affected by resistive defects. As can be seen, both outputs from Sensors are identical – thus proving that no detection could be possible.

In Fig. 45, it is depicted the execution of the March Test in two different rows of the array (Row 0 and Row 1). The cell in Row 0 is affected by a resistive-bridge defect that connects the bit line and the word line through a pass-transistor (DFB5) with a resistance of 40kΩ. As shown in Fig. 37, this defect only sensitizes faults on

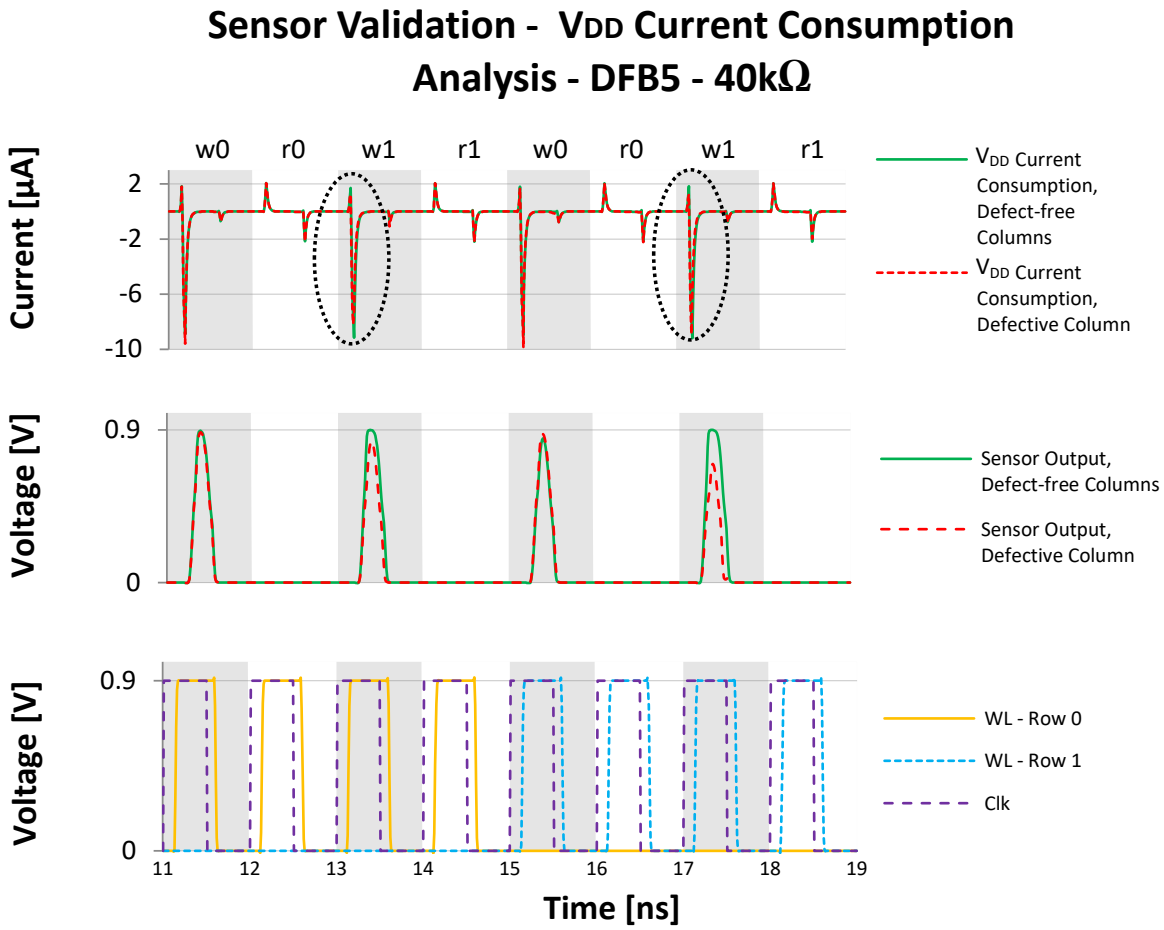


Figure 45: Sensor output when monitoring V_{DD} current consumption.

resistances of approximately 12kΩ or less, and the critical resistance is even smaller when considering only the affected cell. However, by analyzing the current consumption on V_{DD}, it is possible to observe a small discrepancy in the consumption of the defective column. The discrepancy becomes more relevant as the March Test executes operations in other rows rather than the on containing the defective cell, as shown during the $w1$ operation on Row 1 at 17 ns. Even though the analyzed defect is weak (no static nor dynamics faults were sensitized), the sensor is able to generate two distinct output signals.

Fig. 46 shows the sensor output when monitoring the current consumption on GND of a column which the cell on Row 0 is affected by a resistive-open defect between $\overline{Q}$ and the pass-transistor (DFO2) with a resistance of 100kΩ. During the $r0$ operation, it is possible to observe a clear discrepancy in current consumption. Other small discrepancies are observed during write operations, but are not observable in the sensor's output.

4.3.2 Approach 2: Bit Line Voltage Level

The same methodology used to validate the current consumption approach was used to validate the second approach adopted in this work. Fig. 47 presents the simulation

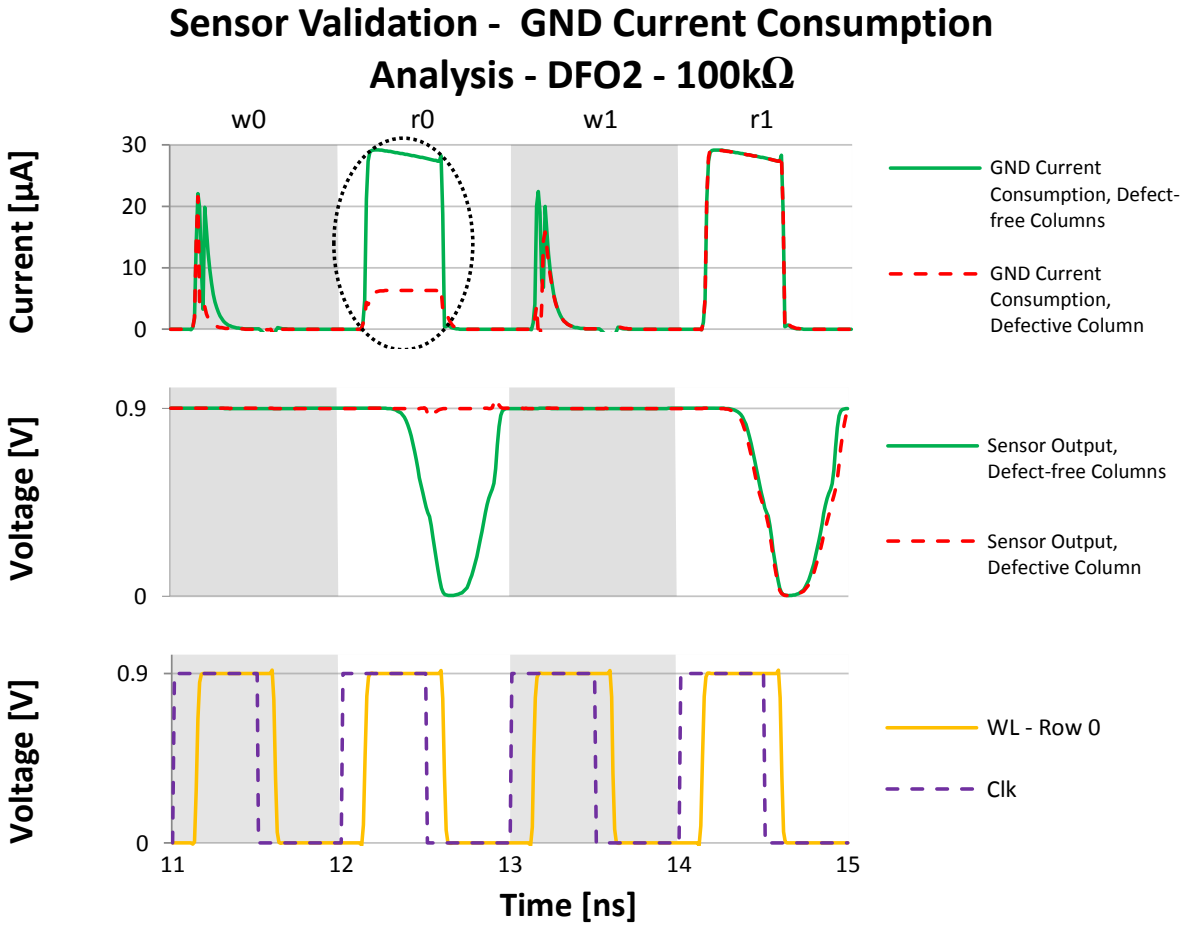


Figure 46: Sensor output when monitoring GND current consumption.

of the BL Sensor while monitoring two distinct columns that have not been affected by resistive defects. As can be seen, both outputs from Sensors are identical – thus proving that no detection could be possible.

Fig. 48 shows the simulation of the March Test on a memory array in which a cell in the first row is affected by a resistive-bridge defect that creates a connection between Q and $\overline{Q}$ (DFB1). The defect has a magnitude of 40kΩ, which is not enough to sensitize any fault. During a $r0$ operation, it it expected that BL will be constantly discharged through the cell. However, as opposing to what is happening with the green signal on the first graph, the BL of the defective column does not discharge as fast as its counterparts. Even though the $r0$ operation is successfully executed, there's still a discrepancy in voltage level of BLs. The sensor is able to correctly generate outputs that identify this discrepancy. The same is observed during the execution of the $w1$ operation.

Validation of the monitoring of $\overline{BL}$s is depicted in Fig. 49, which shows the simulation of a memory array containing a cell on the first row affected by a resistive-open defect between the drain of the pull-down of one of the inverters and GND (DFO3), of magnitude 50kΩ. No functional faults were observed during simulation. Yet, the small

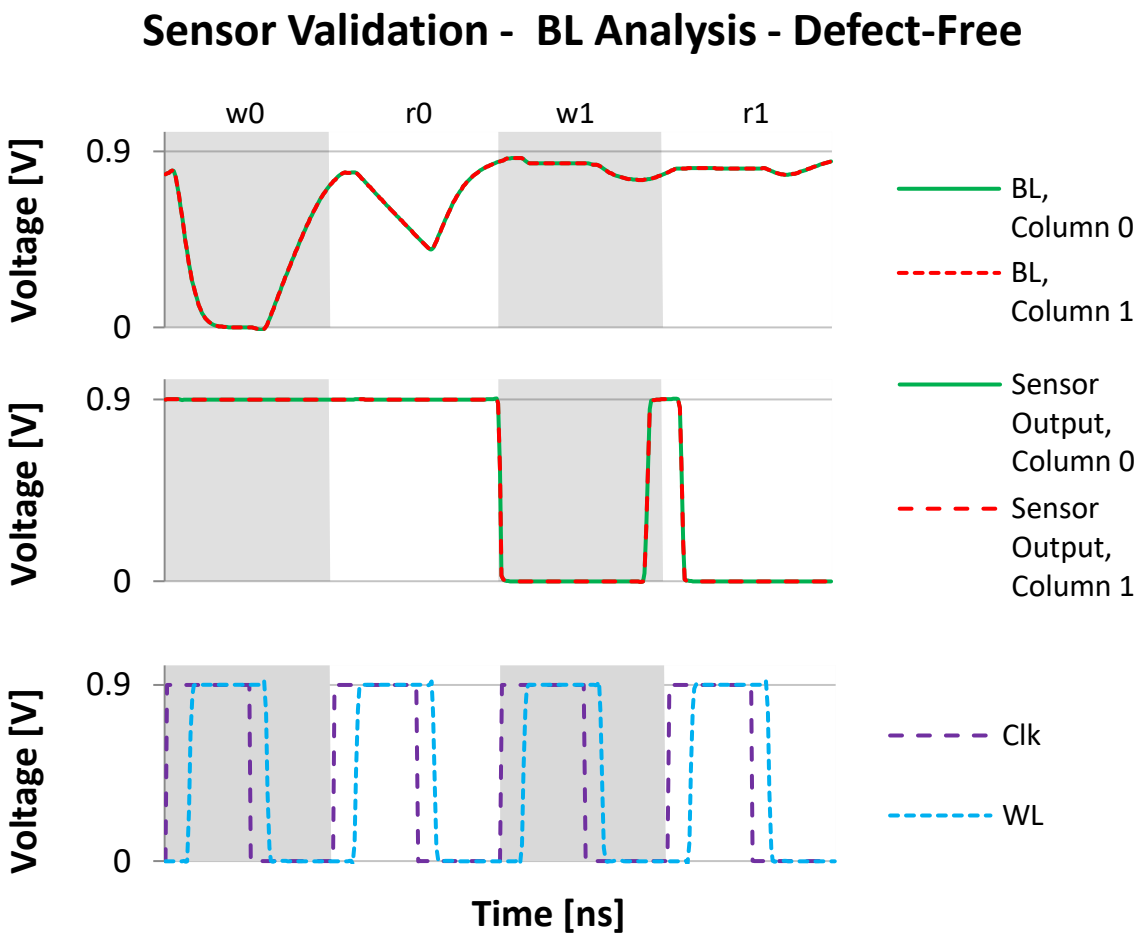


Figure 47: Sensor output when monitoring BL current consumption on defect-free columns.

discrepancy on $\overline{BL}$ during the $w0$ and the more significant discrepancy during the $r1$ operation were enough for the sensor to generate two distinct outputs.

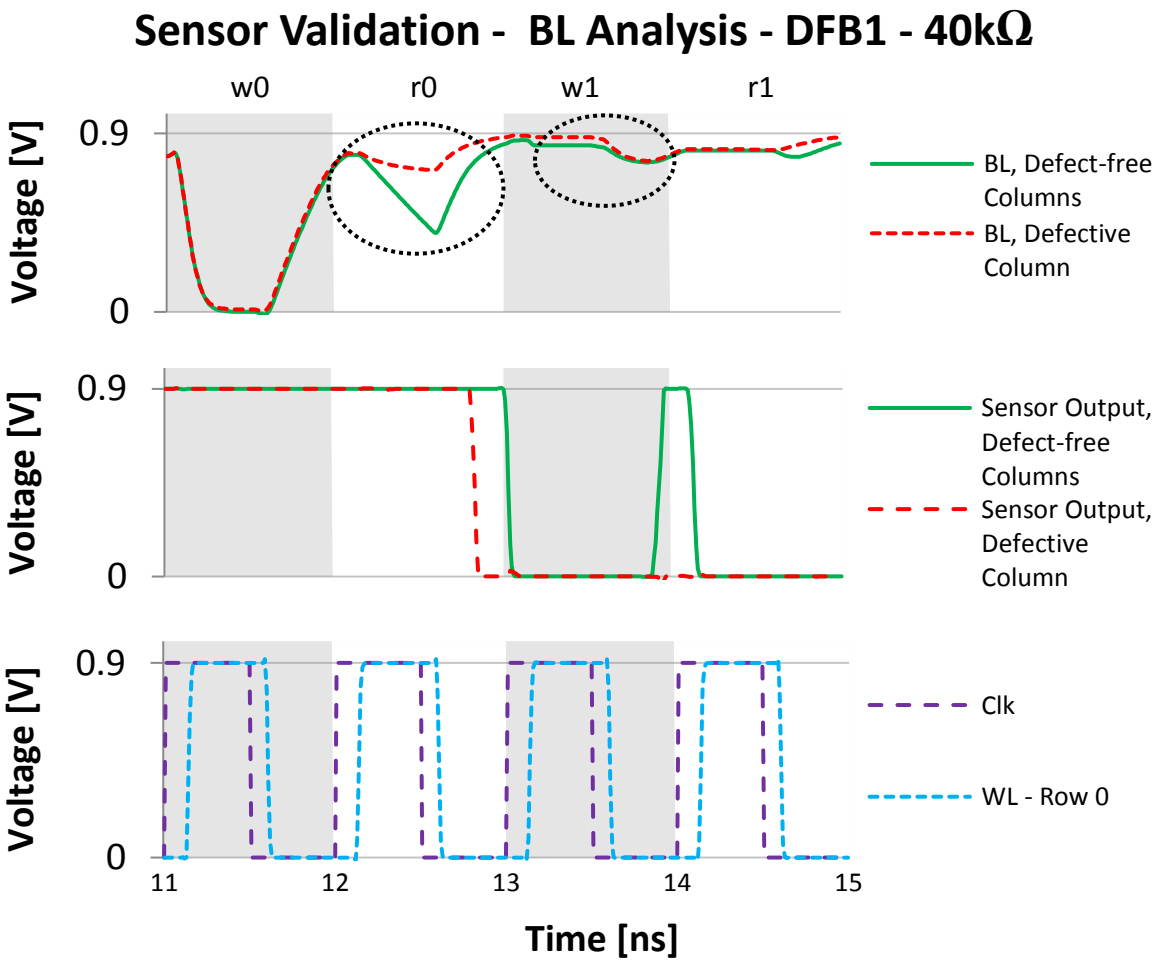


Figure 48: Sensor output when monitoring voltage level of BL.

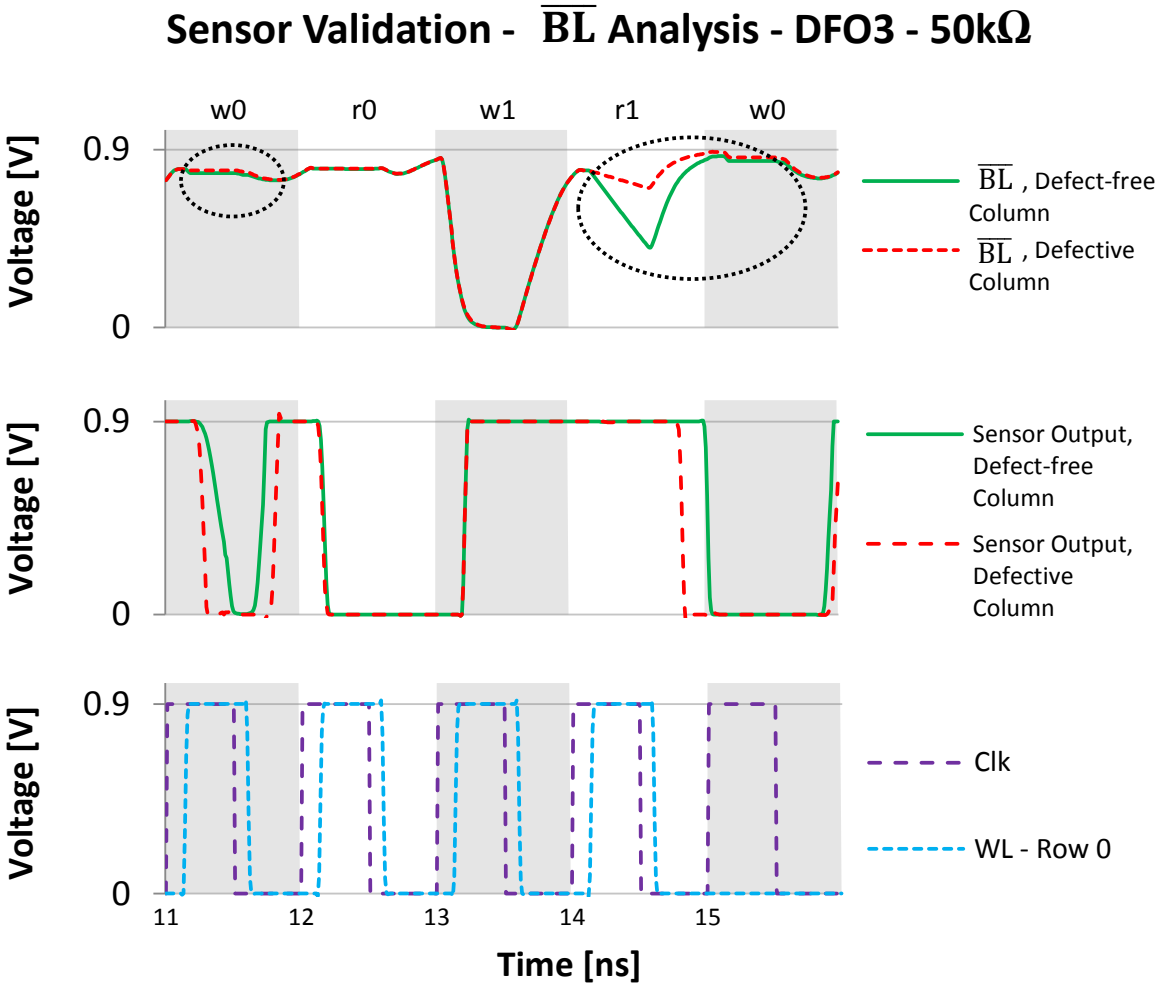


Figure 49: Sensor output when monitoring voltage level of $\overline{BL}$.

5 Results, Discussions, and Evaluations

This Chapter describes the evaluations performed on the memory array and designed sensors. With the memory block and both monitoring strategies validated regarding their functionality, different analysis were carried out in order to asses different characteristics of the circuits regarding faulty behavior, impact of temperature and PV, and costs related to area and power consumption.

5.1 Impact of Temperature on Dynamic Faults

An evaluation on the impact of temperature on dynamic faults was performed. The main goal of this analysis was to investigate how much temperature influenced on the number of consecutive operations necessary to sensitize a fault. A similar analysis has been performed on (HARUTYUNYAN; TSHAGHARYAN; ZORIAN, 2015a). However, the authors limited their investigation to only one exemplar of a resistive-open defect. For this work, all resistive defects that stimulated dynamic faults, open or bridge, were prone to a small window of temperature variation so the impact of temperature of operation could be drawn.

First, it was identified which resistive defects could sensitize dynamic faults on memory cells. Following the results shown on Fig. 37 and Fig. 33, defects DFO2, DF03, DFB2, DFB3, DFB4, and DFB5 (on array impact) were selected for this analysis. Then, memory cells were injected with this set of defects and simulated with different temperatures of operation ranging from 20°C to 35°C. The impact of temperature in the dynamic faults sensitized by these defects is shown in Table 2.

The defect's size was chosen in a way that at nominal temperature (27°C), the defect would sensitize a dynamic fault of two or three operations. The first observation that can be made of these results is that temperature has a different impact on each defect. For DFO2, DFO3, DFB2, and DFB4, an increase in temperature meant an increase in the probability of static faults. The opposite is observed for DFB3 and DFB5, meaning that increase in temperature weakens the defect. This behavior is further discussed in section 5.2, where a more in depth analysis regarding temperature is performed.

The second observation that can be made is the impact of temperature on manufacturing test. For an efficient methodology, it is necessary to test the circuit in different temperatures of operation. For example, consider a methodology that is based on March Test and logic faults detection that is able to detect dynamic faults up to a certain extent. If such test is performed in a memory circuit operating in 20°C, it would report results

Temperature	Defect					
	DFO2 (145kΩ)	**DFO3 (72kΩ)**	**DFB2 (13.7kΩ)**	**DFB3 (45.75kΩ)**	**DFB4 (13.76kΩ)**	**DFB5 (11.79kΩ)**
20ºC	No Fault	No Fault	RDF(2nd)	RDF(2nd)	No Fault	RDF(2nd)
21ºC	No Fault	No Fault	RDF(2nd)	RDF(2nd)	No Fault	RDF(2nd)
22ºC	No Fault	No Fault	RDF(2nd)	RDF(2nd)	No Fault	RDF(2nd)
23C	No Fault	No Fault	RDF(2nd)	RDF(2nd)	No Fault	RDF(2nd)
24ºC	No Fault	No Fault	RDF(2nd)	RDF(2nd)	No Fault	RDF(2nd)
25ºC	No Fault	No Fault	RDF(2nd)	RDF(2nd)	RDF(3rd)	RDF(2nd)
26ºC	No Fault	No Fault	RDF(2nd)	RDF(2nd)	RDF(3rd)	RDF(2nd)
27ºC	DRDF (3nd)	DRDF(3rd)	RDF(2nd)	RDF(2nd)	RDF(2nd)	RDF(3rd)
28ºC	DRDF (2nd)	RDF(2nd)	RDF(2nd)	RDF(3rd)	RDF(2nd)	No Fault
29ºC	DRDF (2nd)	RDF(2nd)	RDF(2nd)	No Fault	RDF(2nd)	No Fault
30ºC	DRDF (2nd)	RDF(2nd)	RDF(2nd)	No Fault	RDF(2nd)	No Fault
31ºC	DRDF (2nd)	RDF(2nd)	RDF	No Fault	RDF(2nd)	No Fault
32ºC	DRDF (2nd)	RDF(2nd)	RDF	No Fault	RDF(2nd)	No Fault
33ºC	DRDF (2nd)	RDF(2nd)	RDF	No Fault	RDF(2nd)	No Fault
34ºC	DRDF (2nd)	RDF(2nd)	RDF	No Fault	RDF(2nd)	No Fault
35ºC	DRDF (2nd)	RDF(2nd)	RDF	No Fault	RDF(2nd)	No Fault

Table 2: Critical resistance values for different temperatures.

completely different than a test performed in 35°C – in fact, the only defect that could be detected by both these tests would be DFB2.

When compared to the results presented in (HARUTYUNYAN; TSHAGHARYAN; ZORIAN, 2015a), it is possible to conclude that the impact of temperature in dynamic faults observed in this work did not have the same relevance as in theirs. This can be explained due to the different technology and methods they used, as they adopted technology models from foundries and used layout simulation to complement electrical simulations.

5.2 Impact of Temperature on Faulty Behavior

The role of temperature on faulty behavior was also evaluated. Three different operating temperatures were simulated : -40°C, 27°C, and 125°C. In defects DFO2, DFO3, DFO4, DFO6, DFB2, DFB4, and DFB5 an increase in temperature worsens the critical resistance, which is defined as the threshold resistance between a fault-free behavior and a faulty behavior. On the contrary, defects DFO1, DFO5, DFB1, DFB3, and DFB6 are more prominent in lower temperatures. The operating temperature affects the critical resistances since the current capabilities of the transistors are also affected. This way, the process of charging and discharging nodes is also affected by the temperature, besides the value of the resistive opens and shorts. It is interesting to notice, that DF4 only manifest a fault at the highest temperature. Table 3 shows the comparison between the critical

DF	Temperature		
	-40°C	***27°C***	***125°C***
DFO1	15.2kΩ (TF)	13.6kΩ (TF)	11.6kΩ (TF)
DFO2	288kΩ (dDRDF)	145kΩ (dDRDF)	72kΩ (dDRDF)
DFO3	134kΩ (dDRDF)	72.5kΩ (dDRDF)	36.8kΩ (dDRDF)
DFO4	-	-	6.2MΩ (dRDF)
DFO5	1.4MΩ (TF)	1.52MΩ (TF)	1.6MΩ (TF)
DFO6	1.84MΩ (TF)	1.82MΩ (TF)	1.60MΩ (TF)
DFB1	47.2kΩ (WRF)	37.6 (WRF)	28.5kΩ (WRF)
DFB2	13.4kΩ (dRDF)	13.7kΩ (dRDF)	14.7k (dRDF)
DFB3	55.0kΩ (dRDF)	46kΩ (dDRDF)	37.8kΩ (dRDF)
DFB4	13.0kΩ (dRDF)	13.65kΩ (dRDF)	15.0kΩ (dRDF)
DFB5	3.6kΩ (IRF)	4.8kΩ (IRF)	5.8kΩ (IRF)
DFB6	12.3kΩ (CFds)	11.4kΩ (CFds)	10.7kΩ (CFds)

Table 3: Critical resistances for different temperatures.

resistances of the three different temperatures of operation when analyzing faults that can only be observed on the defective cell – thus excluding coupling faults.

It is important to state that while a pattern among open defects can be drawn, HSPICE simulations combining temperature and resistances modeling resistive defects may not be a real approximation of reality. When considering temperature, the characteristics of the resistor material has a significant impact on the outcome of the simulation. Thus, the characteristics that the HSPICE simulator uses for its resistors may not represent how resistive defects in memories behave when subject to different temperatures.

5.3 Impact of the Sensor on Faulty Behavior

As stated in the specification of both sensors in Section 3.5, the noise aggregated in the circuit by the sensor is to be considered one of this methodology's drawback. Including the sensor in each column to monitor a designated signal directly affects the cell's susceptibility to faults. Hence, it becomes important to compare critical resistances before and after the introduction of the hardware-based methodology proposed in this work.

The results of this evaluation are summarized in Table 4. The first column presents the results when evaluating critical resistances in the memory array with no hardware-based methodology aggregated. Columns 2 and 3 presents the critical resistances when evaluating faults with the introduction of the current consumption monitoring approach

DF	Approach		
	No Methodology	**Current Consumption**	**Bit Lines' Voltage Level**
DFO1	15.2kΩ (TF)	32.2kΩ (TF)	15kΩ (TF)
DFO2	159kΩ (DRDF)	125.5kΩ (DRDF)	161kΩ (DRDF)
DFO3	80kΩ (RDF)	64.2kΩ (RDF)	80kΩ (RDF)
DFO4	-	-	-
DFO5	1.52MΩ (TF)	2.12MΩ (TF)	1.65MΩ (TF)
DFO6	1.98MΩ (TF)	2.79 MΩ (TF)	2.52MΩ (TF)
DFB1	29 kΩ (WRF)	37.9 kΩ (WRF)	37.6kΩ (WRF)
DFB2	13.5kΩ (RDF)	22.6kΩ (RDF)	13.6kΩ (RDF)
DFB3	45.2kΩ (RDF)	74.3kΩ (RDF)	44.8kΩ (RDF)
DFB4	13.5kΩ (RDF)	17.9kΩ (SAF)	13.6kΩ (RDF)
DFB5	4.8kΩ (IRF)	4.125kΩ (IRF)	4.8kΩ (IRF)
DFB5 (Array)	30.8kΩ (IRF)	27.9kΩ (IRF)	27.9kΩ (IRF)
DFB6	11.4kΩ (CFds)	16.3kΩ (CFds)	11.85kΩ (CFds)
DFB6 (Array)	26.4kΩ(WRF)	22.4kΩ (IRF)	22.4kΩ(WRF)

Table 4: Comparison of critical resistances of static faults between the three circuits addressed in this work.

and bit line voltage level monitoring approach, respectively.

Overall, it is possible to conclude that the second approach has a smaller impact than the first. From the set of defects analyzed in this work, only in three cases the critical resistance had relevant alteration – and in two cases, a stronger defect is necessary to sensitize faults. As for the first approach, all defects had their critical resistance altered and, in most cases, implicated in weaker defects causing faults.

5.4 Defect/Fault Detection

To evaluate the sensor efficiency in generating outputs that can be used to detect resistive defects, a neighborhood comparison detection logic presented on (LAVRATTI, 2012) was inserted in the array. The detection logic, when comparing the signals generated by the sensor, sets a signal to high value whenever a mismatch is detected. Latches are used to store this signal.

However, for FinFET-based memories, this signal may remain in high state for only a short period of time – creating a pulse rather than a square signal. More than that, as the detection logic is purely combinational, a detection may happen during the low stage of the clock, thus causing the latch to not store the value.

This way, instead of using a latch to store the detection result, a D flip-flop with a logic signal of '1' as its input and the detection signal as the synchronization signal

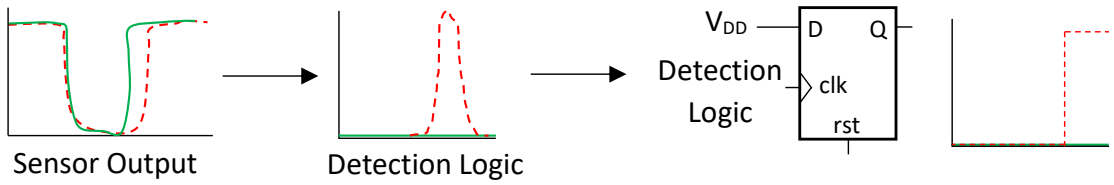


Figure 50: Detection mechanism adopted to evaluate the efficiency of the proposed methodology.

instead of a clock were adopted. Whenever a pulse generated by the detection logic is wide enough to trigger the flip-flop, it outputs a high signal. A reset signal was then used to clear all flip-flop states during a defined moment of operation. Fig. 50 illustrates this sequence of events. The dashed red line represents the output from a column with a defective cell, while the continue green line represents the other defect-free columns in the compared neighborhood.

Thus, to evaluate the sensor's ability to produce efficient results, it was developed an automated tool to detect changes on the output of the flip-flops storing the results from the detection logic. An example of the tool's report can be seen in Appendix C. As a metric of evaluation, it was desired that the sensor could forward to the detection logic signals that could trigger a detection when affected by defects that are half or twice the size of the critical resistance, depending if the defect analyzed is a resistive-open or resistive-bridge.

The results obtained from this evaluation are shown in Table 5. It is important to emphasize that these results were obtained in simulations performed in nominal temperature of operation. For each approach in this work, Table 5 shows the critical resistance of each defect, and the resistance that a defect was first detected. To define this resistance, defects 100 times weaker than the critical resistance were inserted. In each iteration, the strength of the defect was slightly increased, which means that resistance for RO defects was increased while for RB defects resistances was decreased. Each defect was iterated 100 times, in a total of 1200 simulations. For some defects, detection was already possible when the weakest defect for this evaluation was injected. In Table 5, an asterisk identifies these occurrences.

From these results, it was observed that, for all defects, the sensor is able to generate valid results. For the current consumption approach, the hardest defect to detect was DFB5. Detection was only possible on defects with magnitude of 40kΩ or lower, which is close to the critical resistance of 27.9kΩ. This was the only case that the sensor was not able to generate distinct outputs for defects half the strength of critical resistances.

It is also important to state that during this evaluation performed on nominal temperature of operation, no false-positives were detected.

DF	Approach			
	Current Consumption		Bit Lines' Voltage Level	
	Critical Resistance	First Detection	Critical Resistance	First Detection
DFO1	32.2 kΩ	3.85 kΩ	15 kΩ	1.8 kΩ
DFO2	125.5 kΩ	1.3 kΩ*	161 kΩ	1.65 kΩ
DFO3	64.2 kΩ	1.4 kΩ*	80 kΩ	850 Ω*
DFO4	-	1.6 kΩ	-	8.5 kΩ
DFO5	2.12 MΩ	82 kΩ	1.65 MΩ	51 kΩ
DFO6	2.79 MΩ	20 kΩ*	2.52 MΩ	26 kΩ*
DFB1	37.9 kΩ	3.6 MΩ*	37.6 kΩ	828 kΩ
DFB2	22.6 kΩ	2 MΩ	13.6 kΩ	216 kΩ
DFB3	74.3 kΩ	4.9 MΩ	44.8 kΩ	546 kΩ
DFB4	17.9 kΩ	1.7 MΩ*	13.6 kΩ	492 kΩ
DFB5	27.9 kΩ	40 kΩ	27.9 kΩ	2.5 MΩ*
DFB6	22.4 kΩ	1.28 MΩ	22.4 kΩ	2.4 MΩ*

Table 5: Critical Resistances and detection efficiency for both approaches.

An issue can be explored from the results shown in Table 5. In almost all cases, the sensor was able to generate distinct signals for cells affected by very weak defects – defects that are far from sensitizing any functional faults. In this work, it was exploited the sensor's ability to generate distinguished outputs for defective cells regardless of the defect size. However, in industry applications, it is not effective to identify these cells with the purpose to apply replacing techniques as they will never cause reliability issues.

This brings another issue to discussion. There are studies that show the impact of weak resistive defects in memory cells when subject to other reliability issues like Single Event Upsets (SEUs) and Negative Bias Temperature Instability (NBTI) (MEDEIROS; POEHLS; VARGAS, 2016; MARTINS et al., 2016). However, both studies were performed using planar technologies. Thus, new studies to explore the impact of these factors in defective FinFET-based memory cells are necessary to draw a conclusion on at what point exactly a weak resistive defect becomes a reliability issue.

5.5 Impact of Temperature on the Sensor's Output

Throughout the evaluation of defect/fault detection, a detection logic circuit proposed in (LAVRATTI, 2012) was aggregated alongside the sensor proposed in this work. When validating this circuit, it was observed that the output of the sensor (which is the input of the detection logic) suffered from inconsistencies that are not entirely clear. In the output of the PWM stage (and thus the overall output) of the proposed sensor, the output of defect-free columns would vary drastically, causing the detection logic to

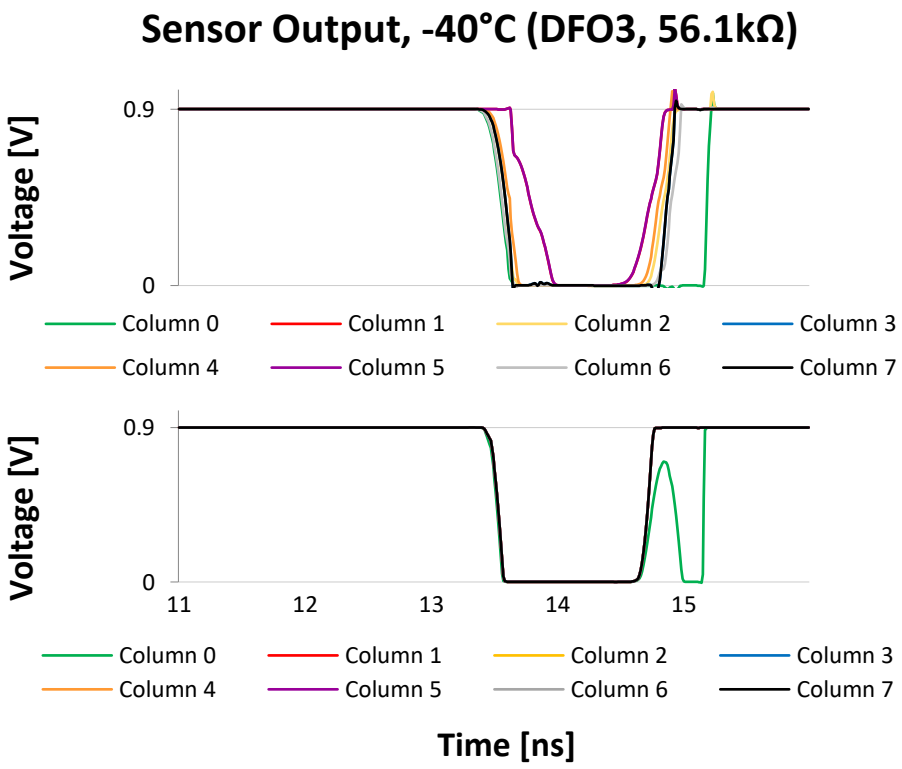


Figure 51: Sensor's output in the presence and absence of a detection logic circuit.

identify false defects in defect-free columns.

This behavior aggravated when evaluating detection capabilities in different temperatures of operation other than the nominal. While there were little concerns for high temperatures, low temperatures caused an expressive discrepancy among the sensors' outputs on both approaches. Fig. 51 shows this behavior. It shows the simulation of a memory array where one of the cells in Column 0 is affected by a defect DFO3 of magnitude 56.1kΩ, which is not strong enough to sensitize faults in a temperature of -40°C. In the first simulation, the detection logic is inserted into the circuit. In the second simulation, the detection logic is removed from the circuit. On both graphs, it is possible to observe that Column 0 has a different output than other columns. Thus, a defect on this column is detected. However, on the first graph, there is a discrepancy among columns that are not affected by any defect. As they are identical columns, it is expected that the sensor outputs the same signal from these columns (as observed on graph 2). Yet, this is not the behavior observed. This inconsistency is detected by the detection logic, which set flags of detection for several of these columns.

While sensors for both approaches were accordingly dimensioned so that these behaviors were not observed in nominal temperature when detecting defects/faults using the detection logic circuit proposed in (LAVRATTI, 2012), it was not possible to perform an automated analysis on the sensor performance considering temperature variations as the detection logic circuit would identify many false positives instances. It is believed that

this behavior is mainly caused by the capacitance aggregated with the inclusion of the detection logic. However, this explanation is not sufficient to understand why the output of seven identical columns (Column 1 to Column 7) vary among themselves. Analyzing the output of each stage of the sensor, it was observed that the two-stage operational amplifier generated the exact same signal for these identical columns – which means that the inconsistent behavior was generated after the PWM stage of the sensor. A more in-depth study regarding the capacitance of FinFET logic gates and their behavior on different temperatures is necessary to drawn a better conclusion.

Due to these issues, it was not possible to evaluate detection capabilities for different temperatures of operation using the proposed detection logic circuit proposed in (LAVRATTI, 2012). Thus, a smaller pseudo-detection circuit was used to evaluate the sensors' capabilities to generate outputs that can be used to detect defects. Rather than monitoring all columns, this circuit monitors only two columns: one that is defective, and one that is not. If there is a discrepancy between the monitored signal of these columns, the circuit flags a signal indicating the presence of an inconsistency. This signal is then used to perform an automated sweep for different magnitudes of the set of 12 resistive defects. For both approaches, it was analyzed how the sensor would operate in a set of 11 different temperatures ranging from -40°C to 125°C.

Before this analysis, sensors from both approaches were dimensioned so that detection in nominal temperature would be possible. After the validation that was discussed on section 4.3, the impact of temperature on these sensors were evaluated.

The evaluation on both approaches used the same methodology. First, it was defined a discrete set of defect "levels". These levels represented discrete steps compared to the critical resistance of the defect on nominal temperature and considering the noise aggregated by the sensor. Levels were determined in a manner that both resistive-open and resistive-bridge defect have the same interval of resistances swept during evaluation. In summary, they were defined by the following rules:

- For **Resistive-Open Defects**, critical resistance in nominal temperature was divided by the number of steps. The result was defined as Level 1, while next levels represented the incremental sum of this result. This way, the resistance of a certain defect of Level M is defined as $M * (CR/S)$, where CR is the critical resistance of this defect and S is the amount of steps adopted. Thus, the interval of resistances between Level 1 and Level S is $CR - (CR/S)$;

- For **Resistive-Bridge Defects**, another method had to be used so that the interval of resistances analyzed between both types of defects were the same. First, an interval was estimated as the analyzed defect was an RO: $CR - (CR/S)$, where CR is the critical resistance on nominal temperature, and S is the amount of steps. Level 1

was then defined as the critical resistance added up with this interval, and following levels represented decrements of Level 1 by (CR/S). This way, the resistance of a certain defect of Level M is defined as $CR + (CR - (CR/S) * M)$.

As no faults were observed for DFO4 in nominal temperature of operation, the adopted critical resistance for this defect was 50kΩ. In Subsection 5.5.2 and Subsection 5.5.1, a table containing the resistances for each level for each defect is presented. It is important to note that in some cases, rather than detecting a defect, a fault is being detected due to the change in critical resistances when varying temperature of operation.

It is essential to emphasize what are the goals with this evaluation. As this is a manufacturing test methodology, it is assumed that the temperature of operation during the test can be controlled. Thus, the results obtained considering a small range of temperature are enough to validate the proposed methodology. An evaluation considering a wide range of temperature aims to not only investigate the impact of temperature on the final results, but also to observe the behavior of several aspects of both approaches such as power consumption and voltage level of bit lines in different temperature setups. More than that, this evaluation can also be used for future projects that aim to use the proposed sensor for online monitoring.

Particular behaviors observed in each approached are discussed in the following sections. Some of the results present may be different from the ones observed in section 5.4 as methodologies adopted to identify discrepancies were different.

5.5.1 Approach 1: Current Consumption

The first approach presented in this work consists of monitoring current consumption in each column of the array to identify surges or declines in consumption. To evaluate the impact of temperature on the behavior of the sensor, one must be aware of a very critical aspect of electronics: as the temperature increases, so does power consumption. When designing a sensor to monitor current consumption, one must be aware to design it to operate in a specific range of temperature – and as this range gets wider, more complex it becomes to achieve efficient results.

Specially in this approach, identifying discrepancies in extreme temperatures becomes a complicated task. In most of the defects analyzed, V_{DD} consumption of defective and defect-free columns becomes similar in low temperatures, while in high temperatures GND consumption of defective and defect-free columns becomes alike. This behavior is shown in Fig. 52 and Fig. 53. The first one shows the current consumption on V_{DD} on a defective column and a defect free column. The shaded area represents consumption on nominal temperature (27°C), while blue lines represent temperatures below nominal and red lines represent temperatures above nominal. Analyzing the behavior of the defective

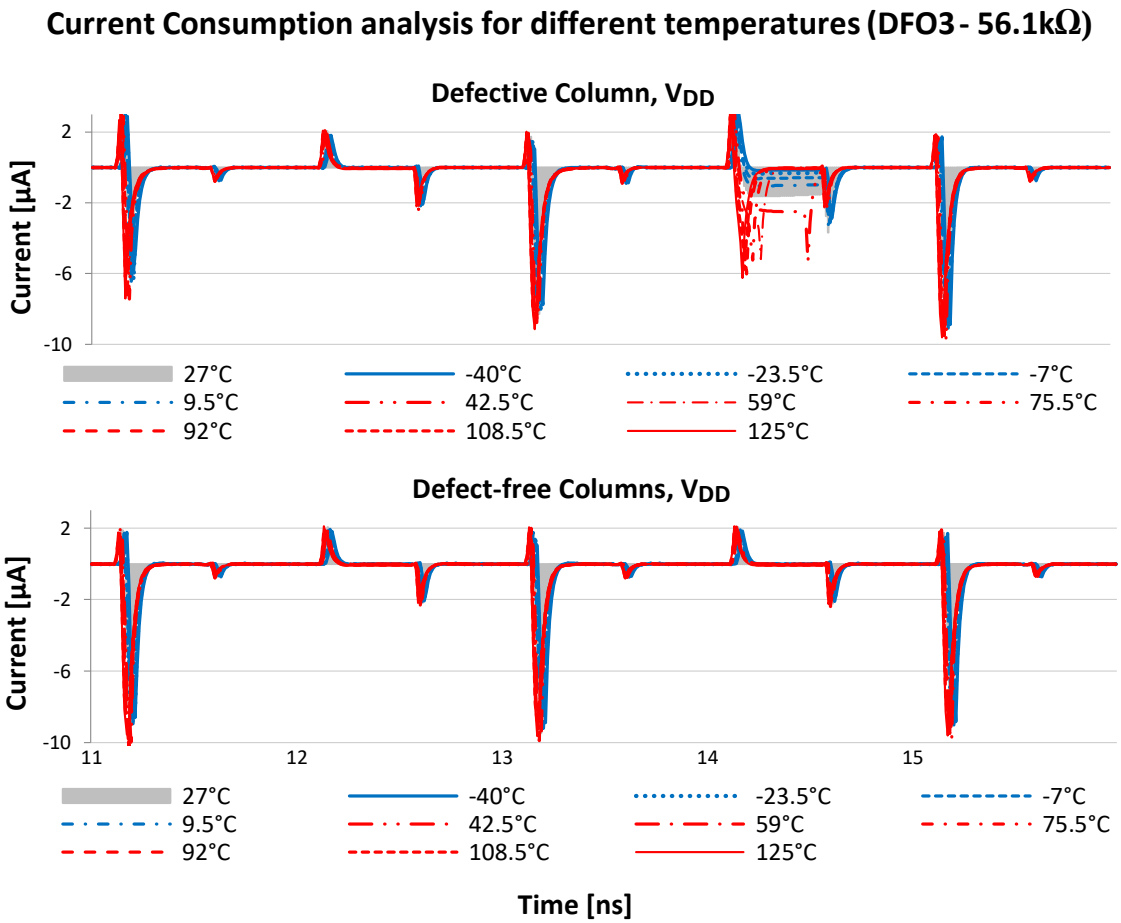


Figure 52: Variation of current consumption on V_{DD} for different temperatures of operation.

column, it is possible to see that current consumption decreases alongside temperature. In negative temperatures, there is little difference in consumption between defective and defect-free columns.

The consumption on GND is shown in Fig. 53. Again, the shaded area represents consumption on nominal temperature (27°C), while blue lines represent temperatures below nominal and red lines represent temperatures above nominal. As previously stated, it was observed that current consumption on GND in defective columns tends to increase alongside temperature, resembling the consumption of defect-free columns. Because of these reasons, it is possible to conclude that the V_{DD} sensor will be more efficient on high temperatures than the GND sensor, while the GND sensor will be more efficient than the V_{DD} sensor on low temperatures. This topic is further discussed in the following paragraphs alongside the results of detection for each sensor.

Before evaluating the sensor on different temperatures, critical resistances for each defect on three temperature corners were defined. Table 6 depicts these results, which assisted the evaluation on whether the sensor was detecting defects or faults. Cells in yellow represent the critical resistance observed in nominal temperature, while cells in

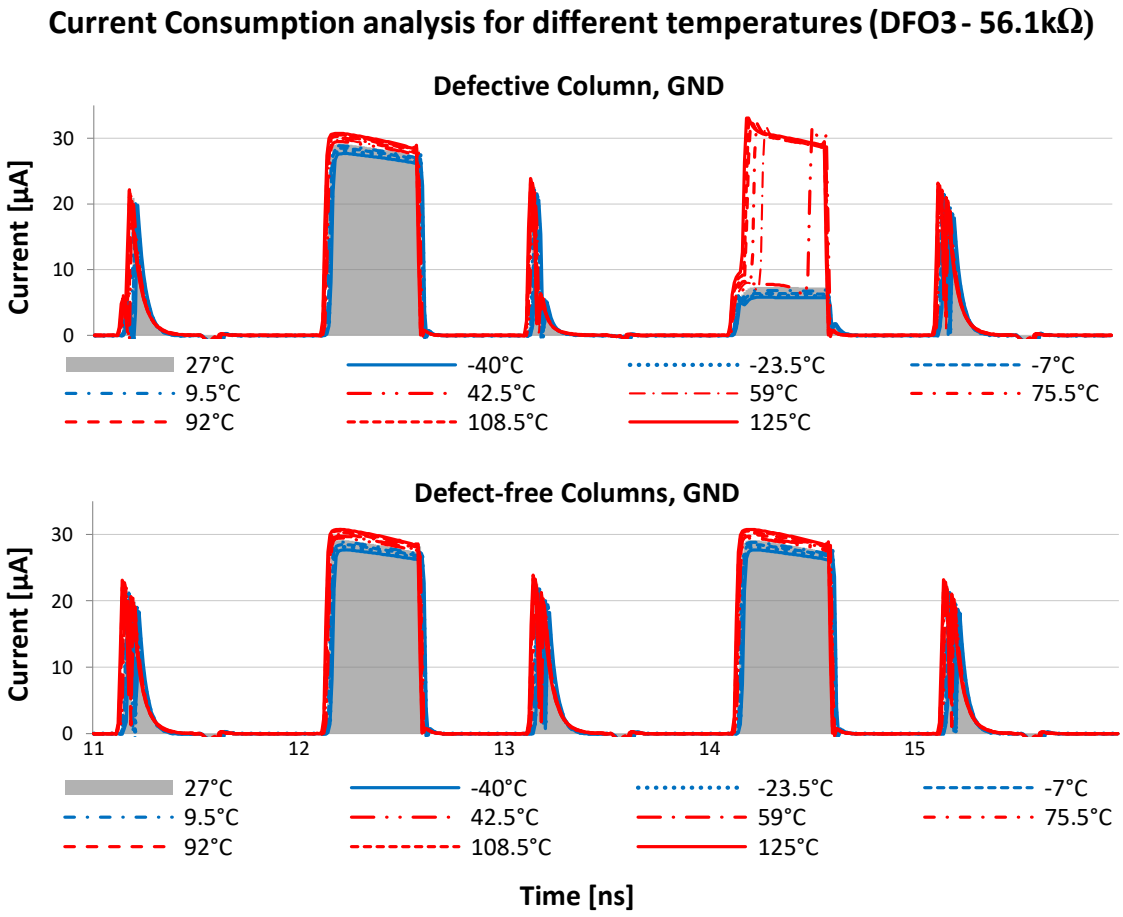


Figure 53: Variation of current consumption on GND for different temperatures of operation.

red represent a deterioration in critical resistance and blues an improvement in critical resistance. Thus, in cases where a critical resistance had deterioration, faults were observed prior to the simulation of Level 10 defects. It is important to emphasize that these are the critical resistances when subjected to stimuli generated by the adopted March Test. Because of this, no dynamic faults are observed. When subjected to other stimuli, defects may sensitize faults in weaker configurations.

With critical resistances defined, it was possible to determine the resistance of each defect level. Due to cost in time of each simulation, it was adopted a total of 10 levels for this evaluation. The resistance simulated for each level and for each defect is presented on Appendix D. Thus, the results presented in the following paragraphs are based on a set of 1320 simulations (10 different resistances, 11 different temperatures, and 12 unique defects).

To evaluate this approach's capabilities to generate distinct outputs in different temperatures, a pseudo-detection circuit that identifies distinct outputs from a defective-column and a defect-free column is inserted into the memory block. Defects' sizes are divided in levels that represent its "strength", where Level 10 represents a defect that is

DF	Temperature		
	-40°C	***27°C***	***125°C***
DFO1	33.5kΩ (TF)	32.2kΩ (TF)	31.4kΩ (TF)
DFO2	274.5kΩ (DRDF)	125.5kΩ (DRDF)	60kΩ (DRDF)
DFO3	131kΩ (DRDF)	64.2kΩ (DRDF)	29.3kΩ (DRDF)
DFO4	-	-	-
DFO5	2MΩ (TF)	2.12MΩ (TF)	2.3MΩ (TF)
DFO6	2.91MΩ (TF)	2.79MΩ (TF)	2.65MΩ (TF)
DFB1	64.8kΩ (WRF)	37.9 (WRF)	36kΩ (WRF)
DFB2	21.9kΩ (DRDF)	22.6kΩ (RDF)	26k (RDF)
DFB3	84.6kΩ (DRDF)	74.3kΩ (DRDF)	63.2kΩ (DRDF)
DFB4	19kΩ (SAF)	17.9kΩ (SAF)	17.0kΩ (SAF)
DFB5	30.8kΩ (IRF)	27.9kΩ (IRF)	25kΩ (IRF)
DFB6	25.8kΩ (IRF)	22.4kΩ (IRF)	18.8kΩ (IRF)

Table 6: Critical Resistance for each defect in different temperatures for the Current Consumption Approach.

able to sensitize static faults in nominal temperature. Thus, Level 10 is represented as the critical resistance of each defect. Table 7 presents the rate of detection for each Level of defect and for different temperatures. First, it is possible to observe high detection rates in nominal temperature and around. From -7°C to 59°C, all defects Level 6 or stronger are detected. For temperatures of 75.5°C and higher, the sensor also presents good results. Table 7 also presents one of the most important aspects of this approach: the inferior detection rate on low temperatures due mostly to the low effectiveness of the GND sensor. This topic will be explored and addresses alongside the results from this sensor in particular.

Table 8 shows the summary of detection rates for each of the resistive-defects analyzed in this work. A detailed version of this table is presented on Appendix D. It can be clearly seen that DFB5 is the most difficult defect to detect. For temperatures higher than 59°C, the discrepancy caused by this defect on current consumption is not great enough for the sensor generate distinct outputs, regardless of the defect's strength. This has a significant impact on detection rate per temperature of operation analyzed, which is shown on Table 9. While detection rates from -7°C to 59°C are acceptable (as they are all above 95%), DFB5 causes these rates to drop to less than 90%. Again, it is also possible to observe by the results in this Table the inferior efficiency of this approach on low temperatures.

Table 10 shows the summary of detection rates for resistive-open and resistive-

	Temperature										
Level	-40 ºC	-23.5ºC	-7 ºC	9.5 ºC	27 ºC	42.5 ºC	59 ºC	75.5 ºC	92 ºC	108.5 ºC	125 ºC
Level 1	33%	75%	92%	92%	92%	83%	83%	58%	58%	58%	58%
Level 2	33%	67%	100%	92%	92%	92%	100%	83%	75%	75%	83%
Level 3	25%	75%	100%	100%	92%	92%	100%	92%	92%	92%	92%
Level 4	17%	67%	100%	92%	100%	100%	100%	92%	92%	92%	92%
Level 5	25%	67%	92%	100%	100%	100%	100%	92%	92%	92%	92%
Level 6	17%	83%	100%	100%	100%	100%	100%	92%	92%	92%	92%
Level 7	25%	75%	100%	100%	100%	100%	100%	92%	92%	92%	92%
Level 8	17%	83%	100%	100%	100%	100%	100%	92%	92%	92%	92%
Level 9	17%	75%	100%	100%	100%	100%	100%	92%	92%	92%	92%
Level 10	17%	92%	100%	100%	100%	100%	100%	92%	92%	92%	92%

Table 7: Overall results on the evaluation of the impact of temperature on the Current Consumption approach.

Discrepancy detection rate each defect – Current Consumption Approach

Defect	DFO1	DFO2	DFO3	DFO4	DFO5	DFO6	DFB1	DFB2	DFB3	DFB4	DFB5	DFB6
Detection Rate	76.36%	87.27%	86.36%	88.18%	100.00%	83.64%	100.00%	90.91%	90.91%	90.00%	47.27%	90.91%

Table 8: Summary of discrepancy detection rate for each of the resistive defects for the Current Consumption approach.

Discrepancy detection rate for different temperatures – Current Consumption Approach

Temperature	-40ºC	-23.5ºC	-7ºC	9.5ºC	27ºC	42.5ºC	59ºC	75.5ºC	92ºC	108.5ºC	125ºC
Detection Rate	22.50%	75.83%	98.33%	97.50%	97.50%	96.67%	98.33%	87.50%	86.67%	86.67%	87.50%

Table 9: Discrepancy detection rate for different temperatures of operation for the Current Consumption approach.

bridge defects. More detailed versions of this table are shown in Appendix D. This table displays a very interesting aspect: even though detection rate is similar, Resistive-Open defects are more likely to cause discrepancies in current consumption than Resistive-Bridge defects. This, consequently, translates in a higher detection rate for ROs than for RBs. A distinguish difference in detection rate can be seen on temperatures higher than 59°C, where ROs have a better detection rate. This is mostly due to DFB5, as it is the most difficult defect to detect by this approach.

The last analysis performed is the efficiency of each sensor separately. As stated previously, detection by GND consumption becomes more complex as temperature rises, while detection by V_{DD} becomes more complex as temperature drops. This behavior can be verified on Table 11 which present detection rates for the V_{DD} and GND sensor. A more detailed table presenting the results for each sensor is shown in Appendix D. On Table 11, it is possible to observe that no discrepancy was detected on -40°C, which means

Discrepancy detection rate for ROs and RBs Defects – Current Consumption Approach

Temperature	-40ºC	-23.5ºC	-7ºC	9.5ºC	27ºC	42.5ºC	59ºC	75.5ºC	92ºC	108.5ºC	125ºC
Detection Rate ROs	23.33%	68.33%	98.33%	98.33%	98.33%	98.33%	98.33%	93.33%	93.33%	93.33%	93.33%
Detection Rate RBs	18.33%	91.67%	100.00%	100.00%	96.67%	95.00%	100.00%	83.33%	83.33%	83.33%	83.33%

Table 10: Summary of discrepancy detection rate for resistive-open and resistive-bridge defects for the Current Consumption approach.

Discrepancy detection rate on different sensors – Current Consumption Approach

Temperature	-40ºC	-23.5ºC	-7ºC	9.5ºC	27ºC	42.5ºC	59ºC	75.5ºC	92ºC	108.5ºC	125ºC
Detection Rate V_{DD} Sensor	0.00%	38.33%	91.67%	85.00%	92.50%	93.33%	90.00%	88.33%	88.33%	88.33%	88.33%
Detection Rate GND Sensor	20.83%	69.17%	95.83%	96.67%	82.50%	78.33%	80.00%	16.67%	2.50%	0.00%	0.00%

Table 11: Summary of discrepancy detection rates on the V_{DD} and GND sensor for the Current Consumption approach.

that current consumption on V_{DD} was similar for both defective columns and defect-free columns. Acceptable detection rates are only reported only temperatures above -7°C. Again, the decrease on detection rate on higher temperatures is due to the complex detection of defect DFB5 and DFB6.

With the results shown in Table 11, it is now possible to address an issue that has been previously pointed out: the low efficiency of the GND sensor. Throughout this work, it has been repeatedly emphasized the difficulties on designing a sensor to monitor signal – specially if this sensor ought to monitor a signal in different temperatures and affected by different hindrances (in this work, 12 different resistive defects). From all the sensors designed for this work, the GND sensor was designed with the smallest current generator to evaluate the relation between current generator dimensioning and efficiency – and as can be seen by Table 11, detection rates for this sensor are not decent. Thus, in order to improve the effectiveness of this approach, a first solution would be refine the dimensioning of the sensor by enhancing the current generator. Other details of these aspects are addressed in section 5.6 and section 5.7.

This retrenchment in the dimensioning of the GND sensor has a direct impact on its efficiency. On a temperature of 75.5°C or above, this sensor becomes nearly useless as it fails to detect almost all of the injected defect.

Finally, it is possible to summarize all results in a Hit/Miss graph connecting detection rate by defect level, as shown in Table 12. Detection rate is around 70% on the weakest defects injected in this evaluation, and grows up to almost 90% for Level 10 defects.

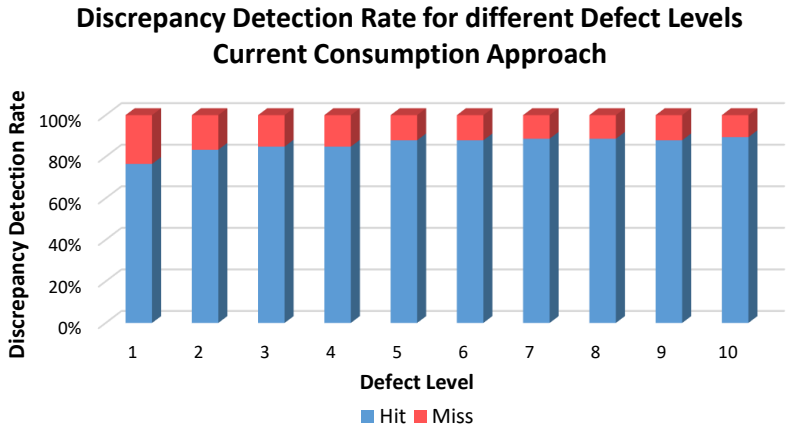


Table 12: Hit/Miss rate based on the size of analyzed defect for the Current Consumption approach.

5.5.2 Approach 2: Bitline Voltage Level

Fig. 54, Fig. 55, and Fig. 56 exemplifies a simulation setup when the adopted March Test is executed on a memory block that contains a defective cell affected by a DFO3 of magnitude 56.1kΩ, which does not cause any faults in nominal temperature. Specifically from 11ns to 16ns, the test is executing $w0, r0, w1, r1$ on Row 0 (which contains a cell affected by a resistive defect) and $w0$ on Row 1. Fig. 54 depicts the variation on bit lines on three distinct temperatures: -40°C, 27°C, and 125°C. In the first graph, it is possible to see that voltage level on the defective's column BL at 125°C is very different from its counterpart in lower temperatures. For this defect, critical resistance tends to become smaller as temperature increases. Thus, in temperatures higher than 75°C, this defect is able to sensitize RDFs. Instead of performing an $r1$, what is actually being performed is an $r0$ as the value in the cell was flipped. This explains the discharging of BL at 125°C.

Fig. 55 and Fig. 56 depicts the sensor's output in the same setup as the former example and are divided in 11 graphs, each representing a different temperature: -40°C, -23.5°C, -7°C, 9.5°C, 27°C, 42.5°C, 59°C, 75.5°C, 92°C, 108.5°C, and 125°C. Over the evaluation of this approach, all defects in different configurations (not strong to sensitize faults, weak, strong) were analyzed to obtain an overall picture of how the sensor behaves when operating in different temperatures. To save space, only the simulation of a weak DFO3 is presented.

The same methodology used to evaluate the first approach was used to evaluate the bitline voltage level approach. First, critical resistances for each defect in three different temperature corners were defined. Again, it is important to emphasize that these are the resistances that cause faults when subjected to the stimuli of the March test adopted in this work. Faults can be observed in weaker configurations of defects when using other sequences of operations. Results obtained in this analysis are shown in Table 13. One

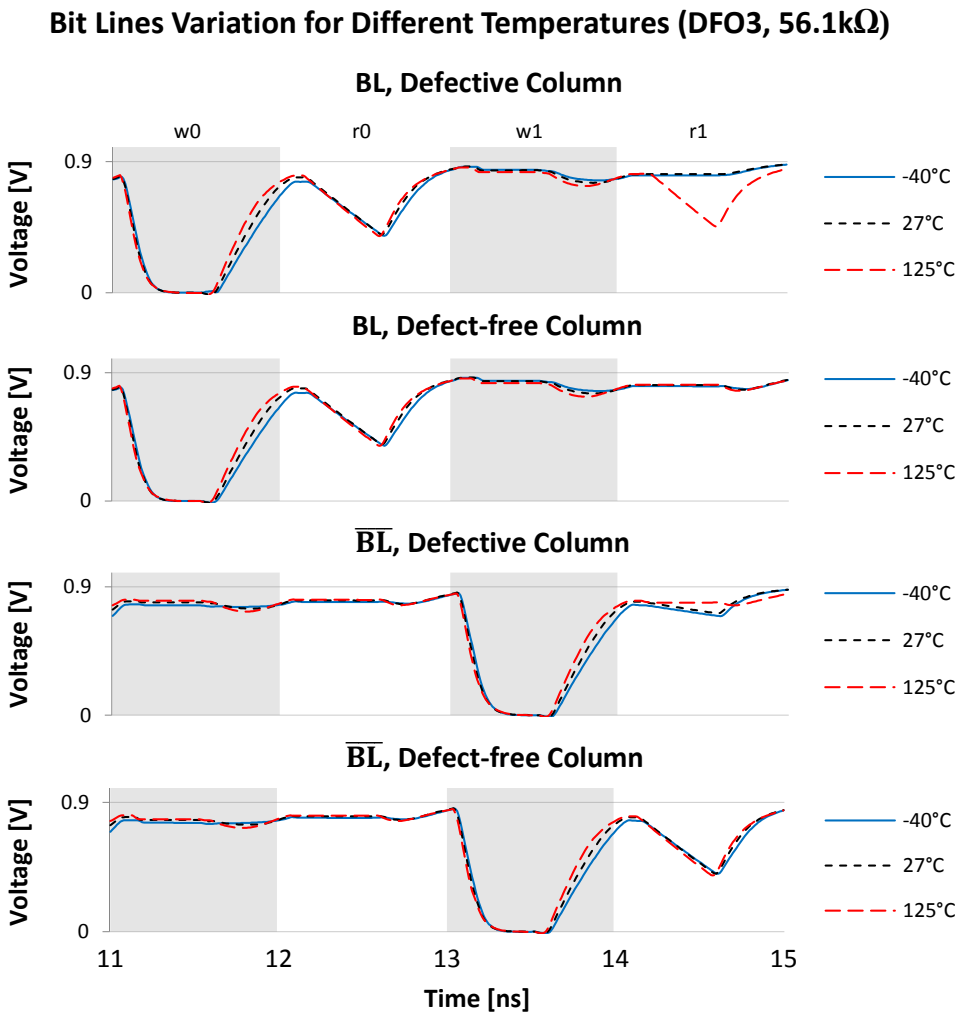


Figure 54: Variation of Voltage Level on Bit Lines considering three different temperature corners.

interesting observation can be made analyzing the results for DFB5 and DFB6. Contrary to all other defects, critical resistances on these two bridge defects improve on both lower and higher temperatures when compared to the critical resistance on nominal temperature. With critical resistances defined, the resistance for each defect Level was defined using the same method previously used. A detailed Table defining the resistance used to simulate each resistive defect and its corresponding Level is presented on Appendix D.

Table 14 presents the overall results obtained when evaluating the sensor's capabilities to output distinguish signals between a defective column and a defect-free column. Each column of the table represents a different temperature, while rows represent the strength of defects, from weaker to stronger. First, it is possible to confirm the proper behavior of the sensor when operating in nominal temperature. Also, the sensor is able to detect all defects and faults at -40°C, -7°C, and -9.5°C. Detection at 42.5°C is also acceptable – degradation in this temperature is caused by DFO1 and DFO4, as will be seen in following tables. It is also possible to observe that while all defects were detected

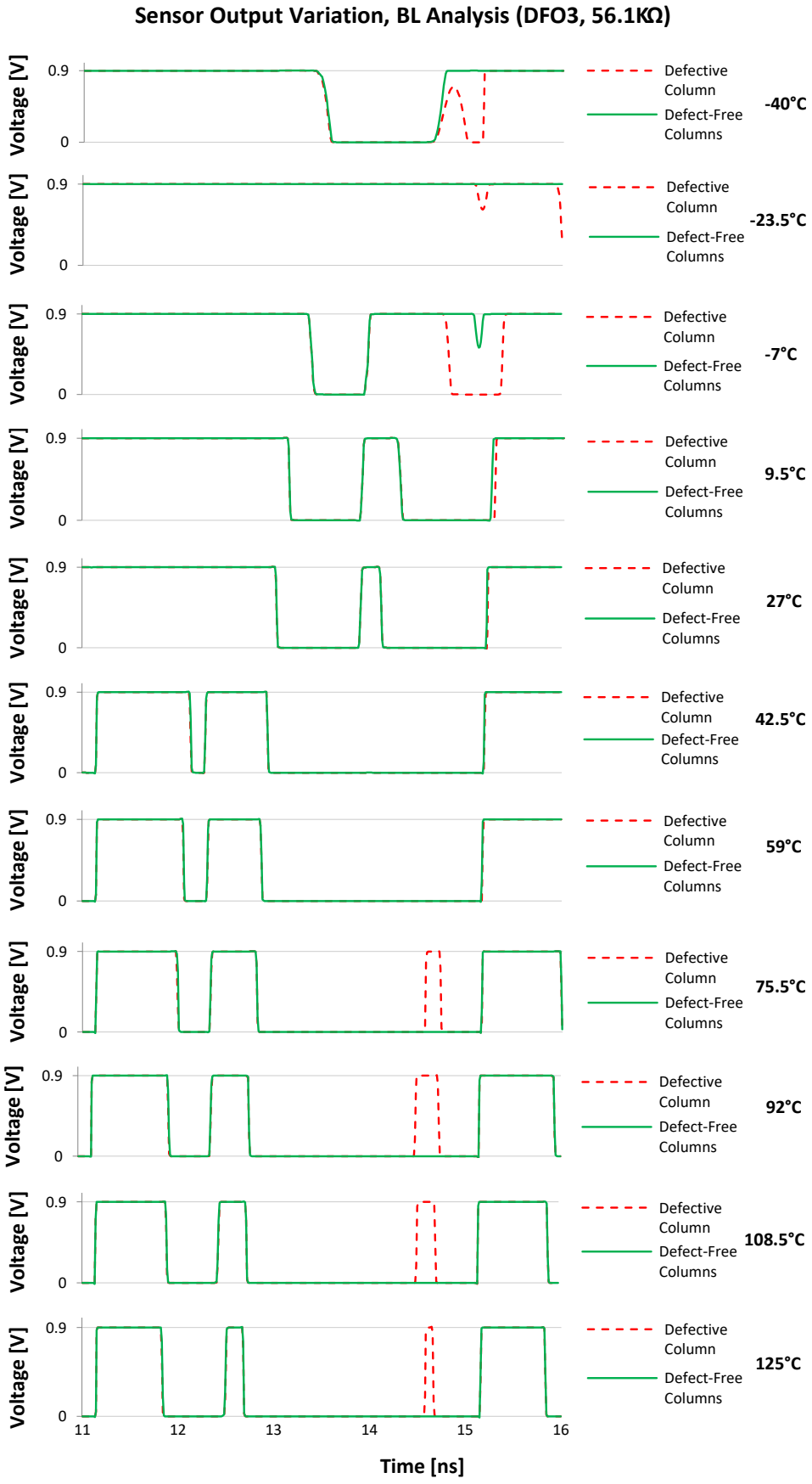


Figure 55: Impact of temperature variation on sensor's output when monitoring BL.

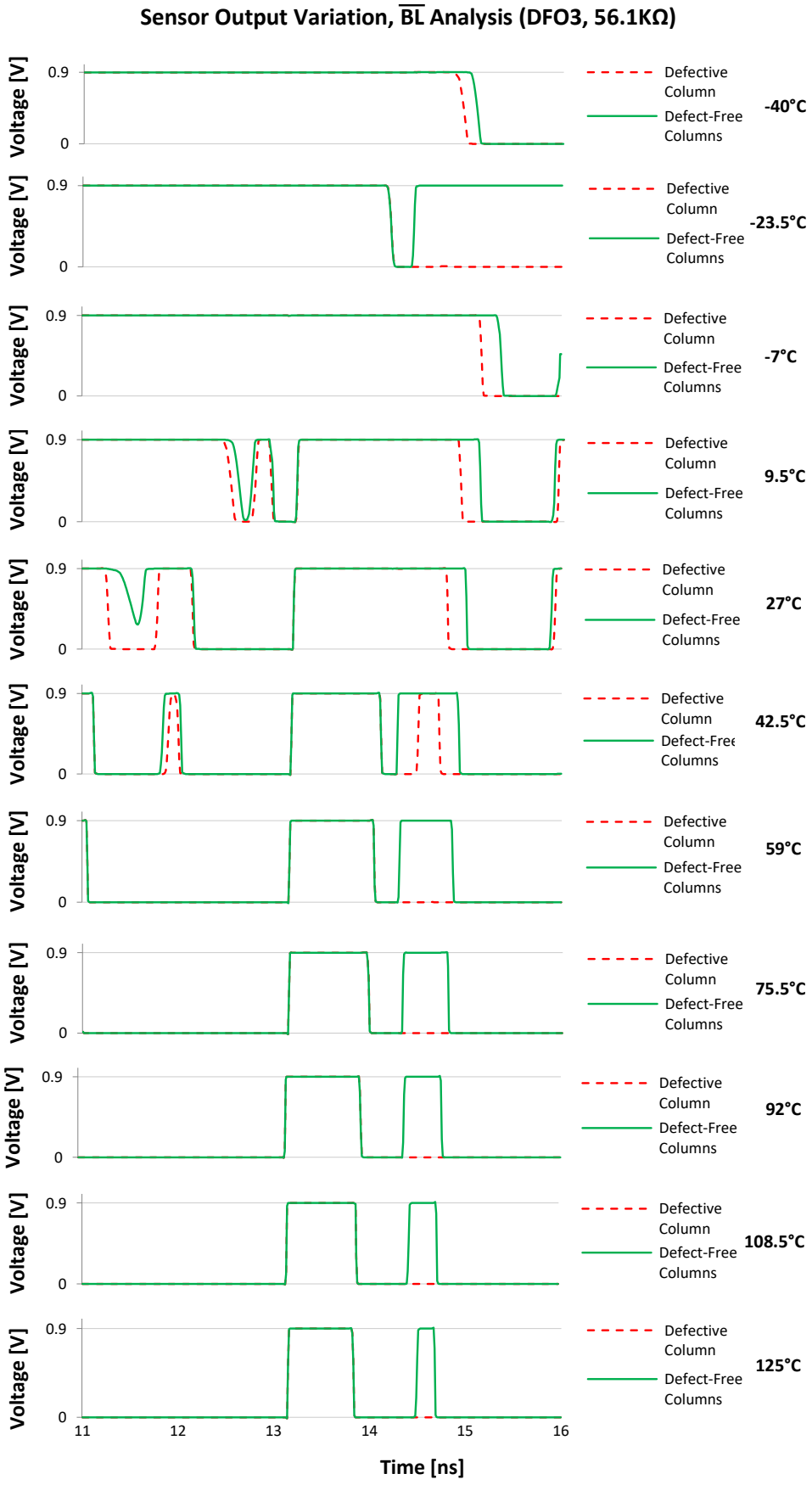


Figure 56: Impact of temperature variation on sensor's output when monitoring $\overline{BL}$.

DF	Temperature		
	-40°C	***27°C***	***125°C***
DFO1	16.6kΩ (TF)	15kΩ (TF)	13.2kΩ (TF)
DFO2	353kΩ (DRDF)	161kΩ (DRDF)	79kΩ (RDF)
DFO3	160kΩ (DRDF)	80kΩ (DRDF)	41kΩ (RDF)
DFO4	-	-	-
DFO5	1.6MΩ (TF)	1.65MΩ (TF)	1.76MΩ (TF)
DFO6	2.73MΩ (SAF)	2.52MΩ (SAF)	2.33MΩ (TF)
DFB1	49kΩ (WRF)	37.6 (WRF)	28.4kΩ (WRF)
DFB2	13.7kΩ (RDF)	13.6kΩ (RDF)	14.5k (RDF)
DFB3	52.5kΩ (RDF)	44.8kΩ (RDF)	37kΩ (RDF)
DFB4	14.7kΩ (WRF)	13.6kΩ (RDF)	14.5kΩ (RDF)
DFB5	25kΩ (IRF)	26kΩ (IRF)	21.6kΩ (IRF)
DFB6	20.3kΩ (IRF)	20.7kΩ (IRF)	15.7kΩ (IRF)

Table 13: Critical Resistance for each defect in different temperatures for the Bit Line Voltage Level Approach.

in -40°C, this is not true for -23.5°C. The next behavior that can be observed by this table is the degradation and then increase in detection as temperature rises. This can be explained by weaker critical resistances in higher temperatures.

From 59°C to 92°C, the sensor is unable to generate distinct outputs for all defects. This is likely due to the sensor calibration to operate on nominal temperature. However, as temperature rises, weaker defects begin to sensitize faults and/or have a more significant impact on bit lines. Only then the sensor is able to generate distinct outputs. In other words, the sensor is detecting not only discrepancies caused by defects, but also discrepancies caused by faults – which are much more prominent and easier to detect.

Table 15 presents the results gathered by defect. Again, columns represent different temperatures of operation, while now rows represent the set of twelve defects analyzed in this work. From this table, it can be clearly seen that there is a subset of defects that have a different behavior to temperature variation: DFO1, DFO4, and DFB3. Although detection rate for DFO6 is not 100%, the results are still acceptable as occurrences of non-detection were observed on defects of Level 1 and 2. Some observations can be made from the set of three defects that have more particular behaviors. First, these defects have a low rate of detection when simulated in -23.5°C, even though their detection rate was 100% for -40°C. Second, all these defects also have low detection rate on the temperature interval of 59°C to 92°C previously discussed. This is more critical in defects DFO4 and DFB3; for temperatures higher than 59°C, defect DFO4's impact on bit lines

	Temperature										
Level	-40ºC	-23.5ºC	-7ºC	9.5ºC	27ºC	42.5ºC	59ºC	75.5ºC	92ºC	108.5ºC	125ºC
Level 1	100%	67%	100%	100%	92%	83%	67%	67%	67%	75%	75%
Level 2	100%	75%	100%	100%	100%	83%	67%	75%	75%	83%	83%
Level 3	100%	75%	100%	100%	100%	83%	75%	75%	75%	83%	92%
Level 4	100%	75%	100%	100%	100%	83%	75%	75%	75%	83%	92%
Level 5	100%	75%	100%	100%	100%	92%	75%	75%	75%	92%	92%
Level 6	100%	75%	100%	100%	100%	92%	75%	75%	75%	92%	92%
Level 7	100%	75%	100%	100%	100%	92%	75%	75%	75%	92%	92%
Level 8	100%	75%	100%	100%	100%	92%	75%	75%	75%	92%	92%
Level 9	100%	83%	100%	100%	100%	92%	83%	83%	92%	92%	92%
Level 10	100%	92%	100%	100%	100%	100%	83%	92%	92%	92%	92%

Table 14: Overall results on the evaluation of the impact of temperature on the Bit Line Voltage Level approach.

	Temperature										
Defect	-40ºC	-23.5ºC	-7ºC	9.5ºC	27ºC	42.5ºC	59ºC	75.5ºC	92ºC	108.5ºC	125ºC
DFO1	100%	10%	100%	100%	100%	60%	20%	20%	20%	60%	80%
DFO2	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
DFO3	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
DFO4	100%	0%	100%	100%	90%	10%	0%	0%	0%	0%	0%
DFO5	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
DFO6	100%	90%	100%	100%	100%	100%	80%	90%	90%	90%	90%
DFB1	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
DFB2	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
DFB3	100%	20%	100%	100%	100%	100%	0%	10%	20%	100%	100%
DFB4	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
DFB5	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
DFB6	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%

Table 15: Discrepancy detection rate for each of the resistive defects for the Bit Line Voltage Level approach.

Temperature	-40ºC	-23.5ºC	-7ºC	9.5ºC	27ºC	42.5ºC	59ºC	75.5ºC	92ºC	108.5ºC	125ºC
Detection Rate	100.00%	76.67%	100.00%	100.00%	99.17%	89.17%	75.00%	76.67%	77.50%	87.50%	89.17%

Table 16: Discrepancy detection rate for different temperatures of operation for the Bit Line Voltage Level approach.

is not great enough for the sensor to generate different signals, regardless of the defect's size. As for the other defects, it is possible to observe an improvement in efficiency as temperature increases. This observation can also be seen on Table 16, which shows the rate of discrepancy detection based on the temperature of operation. There is a significant decrease in efficiency at 59°C, with improved detection rates as temperature increases. It is also possible to observe the poor detection rate on -23.5°C.

Another analysis that can be performed is the detection comparison between

Discrepancy detection rate for ROs and RBs Defects – Bit Line Voltage Level Approach

Temperature	-40ºC	-23.5ºC	-7ºC	9.5ºC	27ºC	42.5ºC	59ºC	75.5ºC	92ºC	108.5ºC	125ºC
Detection Rate ROs	100.00%	68.33%	100.00%	100.00%	100.00%	93.33%	66.67%	68.33%	68.33%	75.00%	78.33%
Detection Rate RBs	100.00%	86.67%	100.00%	100.00%	100.00%	100.00%	83.33%	85.00%	86.67%	100.00%	100.00%

Table 17: Discrepancy detection rate for resistive-open and resistive-bridge defects for the Bit Line Voltage Level approach.

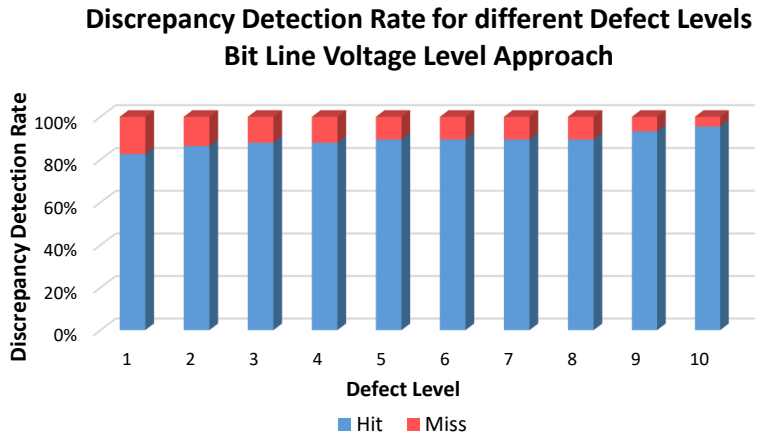


Table 18: Hit/Miss rate based on the size of analyzed defect for the Bit Line Voltage Level approach.

resistive-open and resistive-bridge defects. Table 17 presents the results for this analysis. A more detailed table containing further details of this analysis is presented on Appendix D. Comparing the results, it is possible to conclude that detection of RB defects is an easier task than detection of RO defects. This is likely to the fact that RB defects have a bigger impact on bit line voltage level than RO defects, thus causing the sensor to create distinct outputs more easily, increasing detection rate. It is interesting to observe that the behavior of inconsistent detection at -23°C and from 59°C to 92°C occur on both types of defects.

Finally, Table 18 shows the discrepancy detection rate based on defect size. As expected, this rate increases as defect becomes stronger. Detection rate is 81% for Level 1 defects, and almost 95% for Level 10 defects. Overall, this approach presented positive preliminary results when considering temperature variation. A more in-depth investigation regarding the impact of weak defects on circuit's reliability is necessary to establish if the detection rates presented on this evaluation are acceptable.

5.6 Remarks on the dimensioning of the Current Generator

One of the main stages of the proposed sensor is the generation of a reference current that is used to create a current mirror, which is then supplied to a differential pair of transistors, thus becoming a bias current. In applications in larger technologies (e.g. 65nm), there was not much concern on the dimensioning of this current generator. However, for applications with FinFET transistor, it is necessary to scale this generator in a way that the current generated will be enough to bias the differential pair.

Throughout this work, many configurations of this current generator were designed and tested. From the results obtained within these test, one aspect became clear: the dimensioning of the current generator has a significant impact on the overall performance of the sensor. By designing the current generator using small transistors (transistor using a relative small amount of fins), the bias current is not great enough for the expected operation of the sensor. As the amount of fins used in the current generator is increased, the performance of the sensor improves. However, this also implies in a big cost in area overhead. Overall, if area cost is measured by the amount of fins in the sensor, the current generator occupies more than 65% of total area.

As the main objective of this work was to design a sensor able to monitor signals with very smalls discrepancies, overhead in area was not considered a crucial aspect. In the end, positive results in detection rate were a trade-off with the cost in area. Thus, if one wishes to ignore very-weak defects due to the reasons discussed in section 5.4 and have the smallest impact in area overhead possible, a first approach could be to downsize the current generator, which would consequently narrow the detection interval for each defected.

5.7 Overhead Analysis

To evaluate the costs of the proposed methodology, aspects regarding power consumption overhead and area overhead were analyzed. The following sections detail each of the performed evaluations.

5.7.1 Power Consumption

To estimate power overhead, it was measures power consumption during the execution of a sequence of operations on the three SRAM blocks analyzed in this work: the block with no methodology aggregated, and this same block with the introduction of the two approaches. The sequence of operations performed for this evaluation was the same sequence executed on each row during the March Test adopted in this work: $w0, r0, w1, r1$. Table 19 presents the results of this evaluation; BL approach stands for

Configuration	Consumption (uW)	Overhead
No Methodology	806.63	-
BL Approach	889.46	10.27%
CC Approach	927.34	14.96%

Table 19: Power Overhead of the two approaches.

Circuit	Sensor VDD	Sensor GND	Sensor BL
Converter	1	25	-
Two-Stage Op Amp	77	60	56
Current Generator	190	152	180
Reference	11	10	10
PWM	4	4	4
Total	283	251	250

Table 20: Fins characterization of the circuits that constitute the sensors designed in this work.

the sensor monitoring bit lines' voltage level, while CC approach stands for the sensor monitoring column's current consumption. This results represent power consumption on the entire array (consisted of 1024 rows and 8 columns) plus its peripherals while four consecutive operations are being executed in a single row.

From these results, it is possible to conclude that the approach that causes the smaller impact in power consumption is the bit lines voltage level approach, with an overhead of 10.27%. The current consumption approach has a bigger impact in power consumption, increasing power consumption during the sequence of operations in almost 15%.

5.7.2 Area

As this model library from PTM does not have a cell layout, it is not possible to estimate the area occupied by the sensors. However, it is possible estimate an overhead by considering the amount of fins used for each sensor and comparing it to the total amount of fins in a column. When considering area overhead it is important to have in mind that in each approach, two sets of sensor are aggregated at the same time: in the current consumption approach, a V_{DD} and a GND sensor is used, while in the bit lines voltage level sensor, a sensor is used to monitor BL while another monitors $\overline{BL}$.

As stated on section 5.6, the majority of sensors' area cost comes from current generators. Table 20 shows the amount of fins used for each stage and circuit in each sensor designed in this work. Thus, it is possible to conclude that the sensor that is most likely to occupy the smallest area on a die would be the sensor designed to monitor bit lines' voltage level.

Size	Configuration (Column x Row)	Overhead (CC)	Overhead (BL)
8kbit	1024 x 8	8.691%	8.138%
64kbit	2048 x 32	4.346%	4.069%
512kbit	8192 x 64	1.086%	1.017%

Table 21: Area Overhead of the two approaches for different memory block configurations.

Overall, the current consumption approach uses a total of 534 fins, which is equivalent to 89 SRAM cells used in this work. The bit lines' voltage level uses a total of 500 fins, which is equivalent to almost 84 SRAM cells.

Table 21 presents an estimation in overhead based on the amount of fins used in each approach. For this evaluation, it was considered three different blocks configurations consisted of 1024, 2048, and 8192. For each configuration, the number of fins in each column is defined as the number of rows multiplied by the number of fins in a single cell. With the total number of fins per column defined, an estimation in overhead can be drawn.

From the results presented in Table 21, it is possible to see that the bit lines' voltage level approach has a slightly smaller overhead in area. When compared to other similar methodologies used in larger technologies such as the one presented in (LAVRATTI, 2012), the methodologies presented in this work have a much more significant impact in area.

5.8 A Preliminary Evaluation on Process Variation

In modern ICs, PV represents one of the main challenges in IC design. It can be regarded as discrepancies in transistors' parameters due to inconsistencies during manufacturing. Ultimately, this discrepancies cause deviations in delay, threshold voltage, voltage level, among other key elements that guarantee the proper behavior of the circuit.

As stated in section 2.2, there are two types of PV that have a more meaningful impact: (1) Inter-Die and (2) Intra-Die. The first represents variations among different dies, while the latter represents variations among transistor within the same die. When designing a circuit, one must be aware that any circuit during manufacturing will be prone to these variations.

In this work, a preliminary evaluation on the behavior of the SRAM block and the sensor under PV was carried out to investigate the efficacy of the proposed methodology under the fluctuations caused by PV.

There are many ways to model PV. An approach that is well accepted and used in similar analysis is to perform Monte Carlo simulations using Gaussian distributions to randomly alter parameters. To perform these simulations, the variations of the device pa-

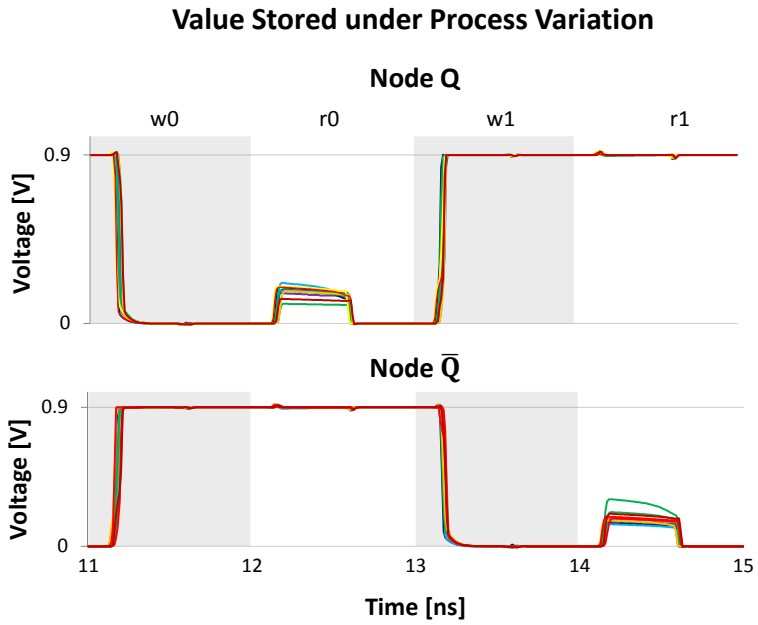


Figure 57: Stored value in a cell in Monte Carlo simulations considering Inter-Die variations for H_{FIN}, and Intra-Die variations for $PHIG$, T_{FIN}, and L.

rameters have been assumed as normal distributed random variables with a 3σ deviation, following specifications from similar works such as (GOMEZ et al., 2016).

Altogether, four parameters were modified during simulations: Fin Height (H_{FIN}), Gate Length (L), Fin Width (T_{FIN}), and Gate Work Function ($PHIG$). To evaluate the degree of variation of parameters, it was analyzed the tolerance of the memory array to the effects of process variation. It was observed that the first three parameters can be varied following the trend of 20% of nominal parameters values also observed in older technologies. However, the Gate Work Function parameter, which is strongly impacted by the granularity of the metal that constitute the gate, does not variate at the same rate. Other works stipulated that this parameter differs from 4% up to 10% of its nominal value (DADGOUR et al., 2010; MEINHARDT, 2014). Thus, for this work, it was defined a value of 5% of variation of nominal value. Fig. 57 presents the internal nodes of a memory cell when subject to Monte Carlo simulations (10 iterations, each one represented by a different color) replicating process variation during manufacturing, considering Inter-Die variations for H_{FIN}, and Intra-Die variations for $PHIG$, T_{FIN}, and L.

5.8.1 Inter-Die Process Variation

In Inter-Die variations all transistors are in the same corner, which means that all transistor have the same exact parameters even though they may differ from the nominal parameters of the technology adopted (which for this work can be seen in Table 1). This type of PV does not have a meaningful impact in the sensor performance as all transistors are still in the same corner. Thus, all columns that are defect-free are still

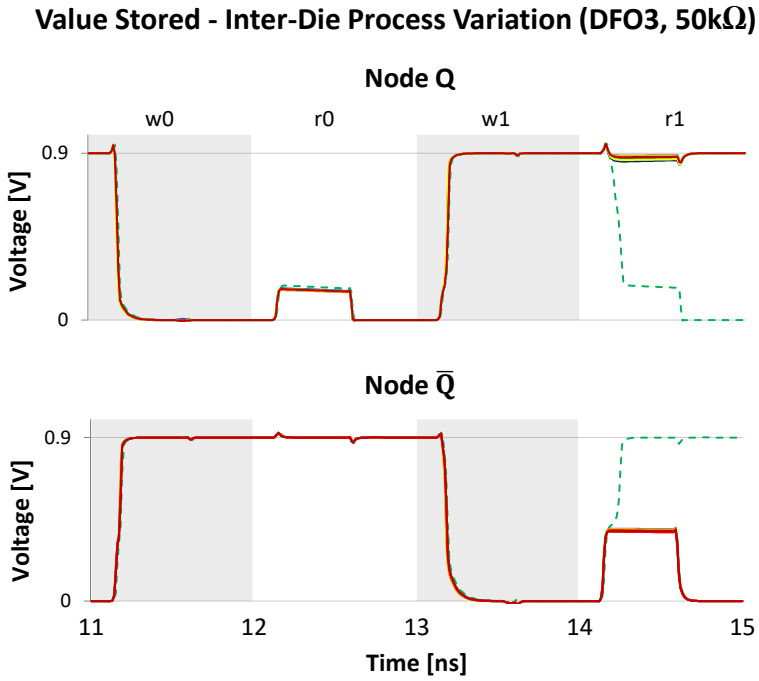


Figure 58: Stored value in a cell affected by a DFO3 in Monte Carlo simulations for Inter-Die Process Variations.

draining the same current and bit lines are still being charged and discharged at the same pace. Consequently, all outputs generated by sensors are exactly the same.

The only impact of this type of PV is the fluctuation in critical resistance. Fig. 58 presents this behavior. It shows the voltage level on nodes Q and $\overline{Q}$ during the execution of the sequence of operations $w0, r0, w1, r1$ on a cell affected by DFO3 of magnitude 50kΩ, which is not enough to sensitize any faults in nominal temperature and without PV. Each color represents an iteration of the Monte Carlo simulation, thus a different set of parameters. It is important to emphasize that in these simulations, all transistors in the same iteration are on the same corner and therefore have the same parameters. From the waveforms in Fig. 58, it is possible to observe that in one of the Monte Carlo simulations (the green dashed line), the cell suffered a destruction during the $r1$ operation. This behavior was not observed on other simulations. For that reason, it is possible to conclude that a cell may be more vulnerable or more resistant to defects based on the corner it was manufactured.

5.8.2 Intra-Die Process Variation

In Intra-Die variations, parameters in each transistor are randomly varied. Thus, it is most likely that no transistor in the circuit is in the same corner. This exponentially increases the complexity of designing a sensor – especially if one aims to monitor signals and detect discrepancies. If no transistor is equal to other, than aspects that rely on

transistors' parameters such as current consumption or the charge and discharge of bit lines will not have a “default" value, which directly affects detection of deviations as everything will be deviated.

In order to verify this behavior, the impact of this type of PV in the circuit was evaluated. Three parameters were altered using Gaussian distributions to randomly alter them following Intra-Die variations: $PHIG$ (5%), T_{FIN} (20%), and L (20%). H_{FIN} was also altered using Gaussian distributions (20%), but following Inter-Die variations as this parameter is most likely to suffer from this form of PV.

The evaluation was divided in four steps: first, it was evaluated how the memory array behaved when subjected to PV behaved and upon aggregating the hardware-based methodologies. In this step, sensors were not be subjected to PV, and their output was be analyzed. In a second step, sensors were subjected to PV, and aggregated to defective, PV-free memory arrays in order to analyze the impact of PV solely on the structure of sensors. Finally, all transistors in the circuit (memory array, peripherals, sensors) were subjected to PV.

5.8.2.1 Approach 1: Current Consumption

Fig. 59 presents the current consumption and the output of sensors in one of the iterations of the Monte Carlo simulations subjecting the block and peripherals to PV. It shows the current on V_{DD} and GND on eight columns (each column represented by a different column). In this evaluation, no resistive defect was injected. Even so, there are significant discrepancies on surges and maximum consumption caused by the variation of parameter, and that have direct impact on sensor output. Consequently, sensors in each column output different signals. This mismatch in signals that are supposed to be identical can be interpreted as the presence of a defect by a detection logic circuit.

The second evaluation for this approach was to analyze the impact of PV solely on the sensor and on the presence of a DFO3 of a magnitude of 50kΩ in the PV-free memory array. Fig. 60 shows an iteration of the Monte Carlo simulation of this evaluation. As transistors in the memory block and peripherals are in the same corner, all sensors on defect-free columns are receiving the same input. This can be verified by the first and third graph on Fig. 60, which shows consumption on V_{DD} and GND. Again, the column affected by a resistive defect is represented by a red dashed line, while defect-free columns are represented by colored lines. The second and fourth graphs show the output of the V_{DD} and GND sensor, respectively. From the V_{DD} sensor output, it can be seen that the output from the defective column is masked with the output from other columns at 0.9 V. It is also interesting to note that the output of some other defect-free columns were 0 V. The same behavior is observed on the output of GND sensor, as it generates fixed signals in 0.9 V for some columns and in 0 V for other columns. For this sensor, it is also

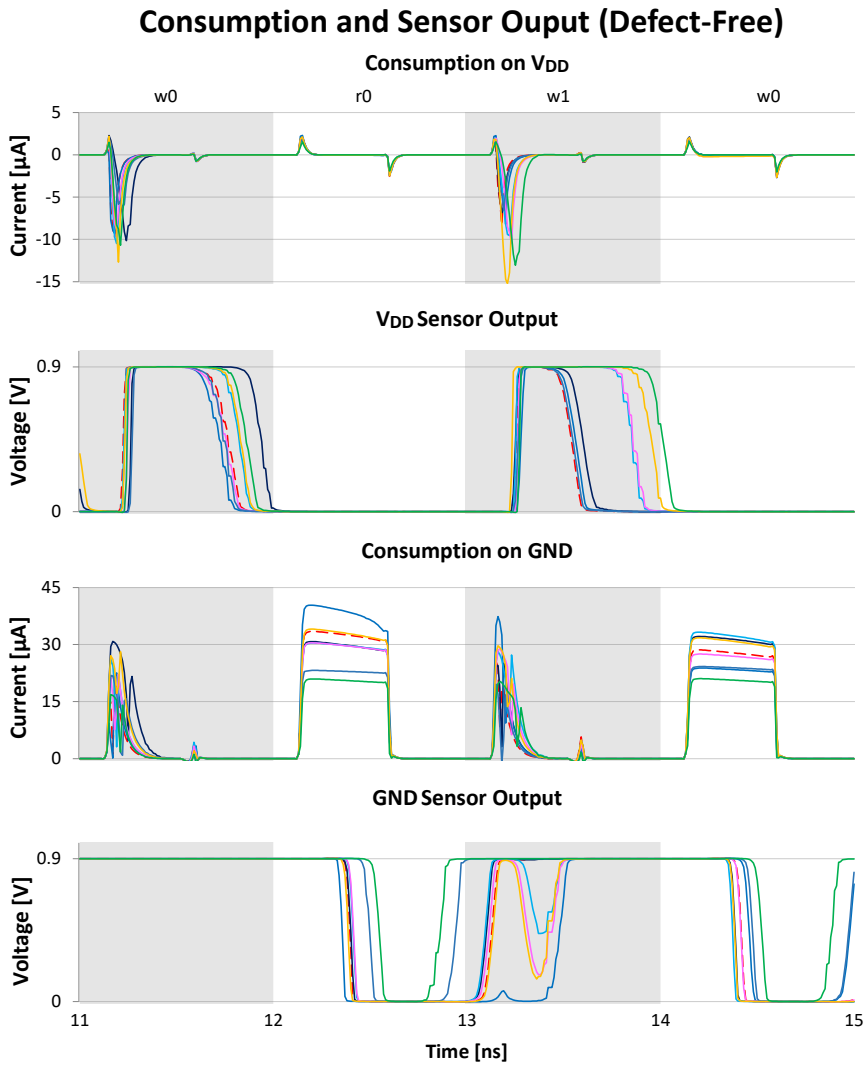


Figure 59: Consumption and Sensor output of an Iteration of the Monte Carlo simulations for the Current Consumption approach altering the memory block and peripherals.

possible to observe the output from a single column (represented by the dark blue line) alternating between nominal voltage and 0 V.

Thus, from the results presented on Fig. 59 and 60, it is possible to conclude that the impact of intra-die PV on the sensor is much more meaningful than the impact on the array and peripherals.

The final evaluation for this approach was to submit all transistor to intra-die PV. Results are shown in Fig. 61, which shows the current consumption and sensors' output in one of the iterations of the Monte Carlo simulation. Likewise previous evaluations, the defective column is represented by the red dashed line, while defect-free columns are represented by other colored lines. The results obtained in this evaluation summarize results observed in previous analyzes: monitoring and distinguishing signals becomes a complex matter when considering intra-die variations due to the difficulties involved in establishing a pattern. Although sensors are able to generate distinct outputs from columns affected

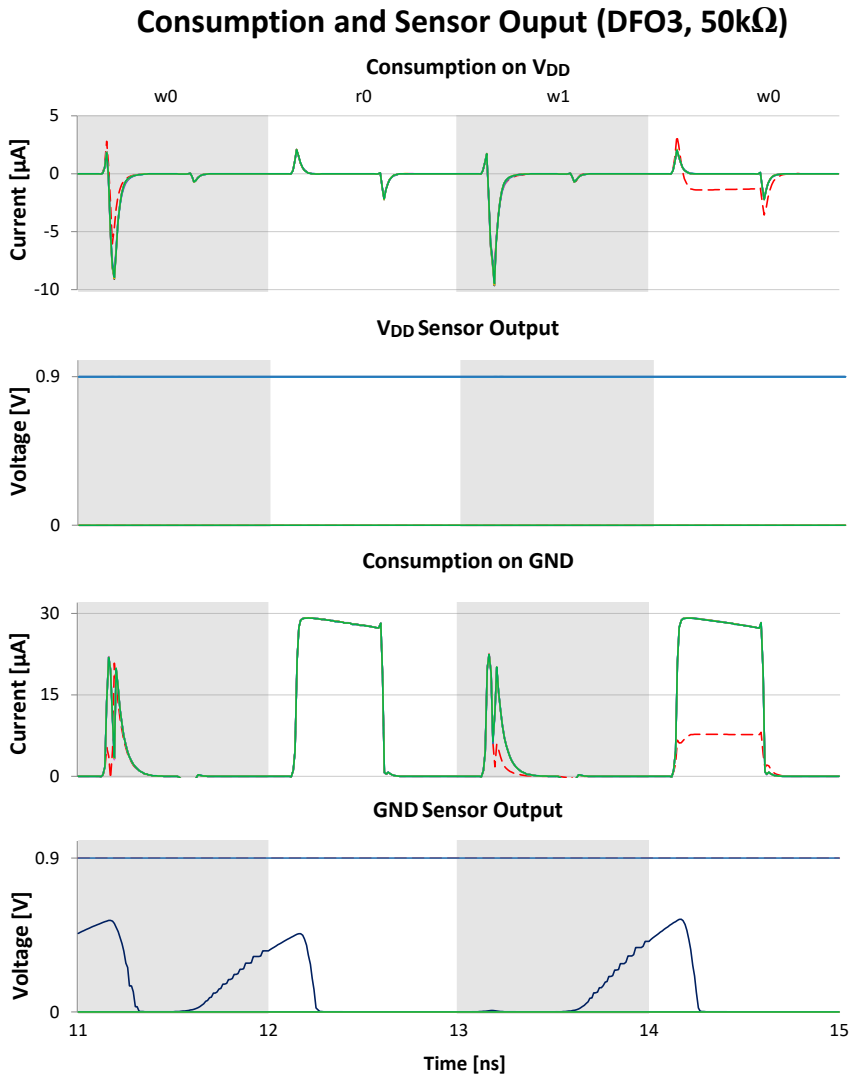


Figure 60: Consumption and Sensor output of an Iteration of the Monte Carlo simulations for the Current Consumption approach altering only sensors.

by resistive defects, the impact of PV on other defect-free circuits is just too relevant. Analyzing the output of the V_{DD} sensor on Fig. 61, it is possible to observe three distinct behaviors from defect-free columns that were identical upon design but suffered altercations during manufacturing: stuck at 0.9 V, stuck at 0 V, and a signal transition from 0.9 V to 0 V represented by the light blue line. With this level of inconsistency, it is doubtless that many defects will not be detected and many false-positives will emerge during manufacturing test.

5.8.2.2 Approach 2: Bitline Voltage Level

In the first evaluation related to the second strategy of the proposed methodology, the memory array and peripherals were subject to PV. An iteration of the Monte Carlo simulation is shown in Fig. 62, which present both BL and $\overline{BL}$ of the memory array consisted of 8 columns, and the output of sensors for each of these columns. In this

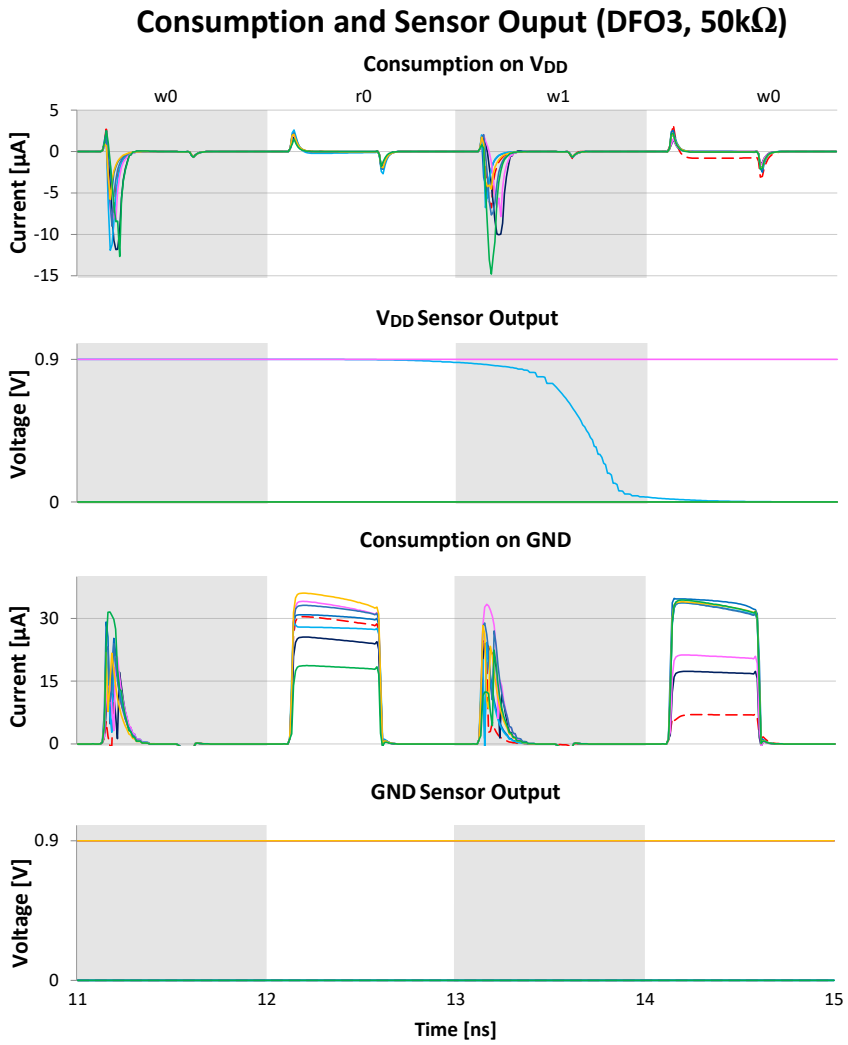


Figure 61: Consumption and Sensor output of an Iteration of the Monte Carlo simulations for the Current Consumption approach altering all transistor in the circuit.

simulation, there are no defective cells. Thus, it should be expected that outputs from sensors should not vary much. However, this is not observed. Even though all sensors are in the same corner, variations caused by PV in the array are already enough to generate distinct outputs in the sensor.

In a second step, it was analyzed the impact of PV solely on the structure of sensors. Memory array and peripherals were maintained in nominal corner, and parameters in the transistors were randomly varied. A DFO3 of magnitude 56.1kΩ was injected into one of the array's cell. Figure 63 shows one of the iterations of the Monte Carlo simulations. The red, dashed line represents the defective column, while each other colored line represents a different defect-free column. As can be seen by the figure, bit lines signals have exactly the same voltage level as there are no variations in the memory array and peripherals. However, process variation on sensors are enough to create distinct outputs, which could be used by a detection logic to indicate the presence of resistive defects and

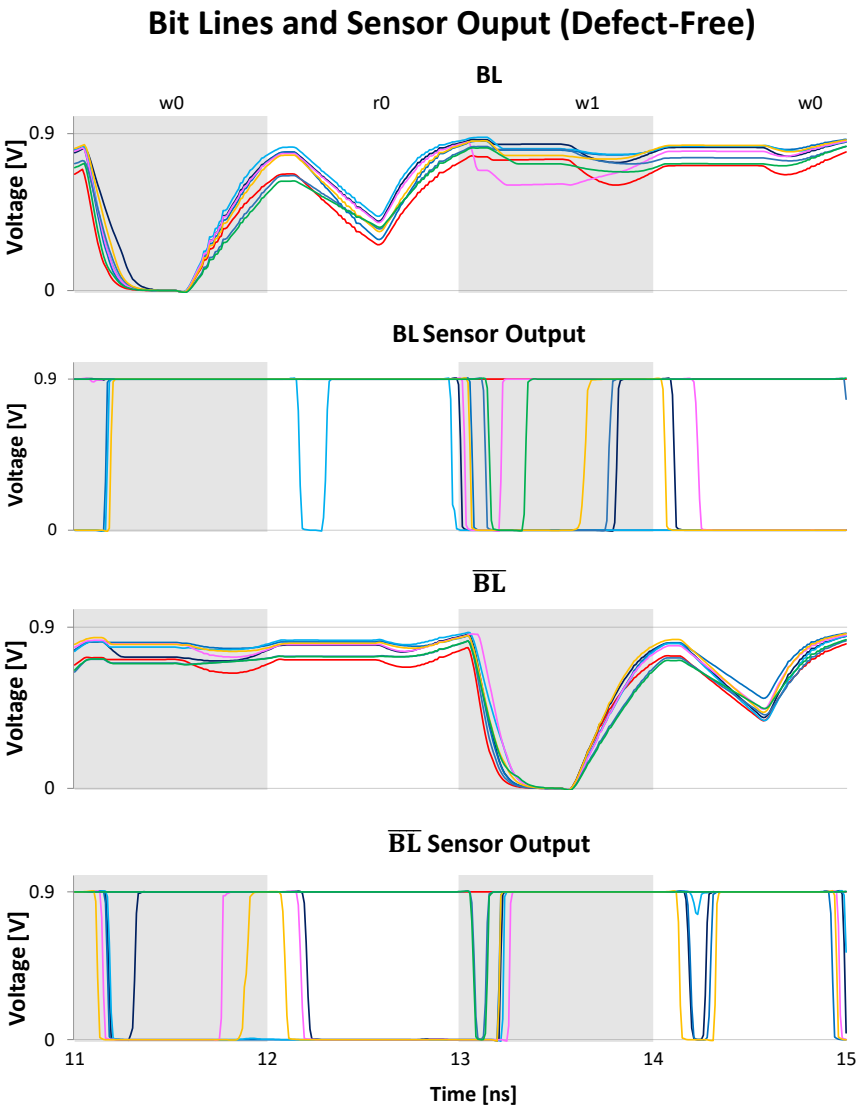


Figure 62: Bit Lines and Sensor output of an Iteration of the Monte Carlo simulations for the Bitline Voltage Level approach altering parameters in the memory block and peripherals.

causing false-positives.

Finally, it was analyzed the impact of PV on all transistors of the circuit, including memory cells, peripherals, and sensors. Fig. 64 presents an iteration of the Monte Carlo simulations. The defective column is represented by the red, dashed-line, while defect-free columns are represented by colored lines. Following the results observed in previous evaluations of this approach, it was not possible to safely identify the defective column. Overall, this approach presented no tolerance to PV, mostly due to sensors' capabilities do produce distinct outputs from small deviations. Even though this is a good aspect when considering capabilities to generate outputs that can be used to detect defects and faults, this also backfires when the instability generated by the manufacturing process is taken into account.

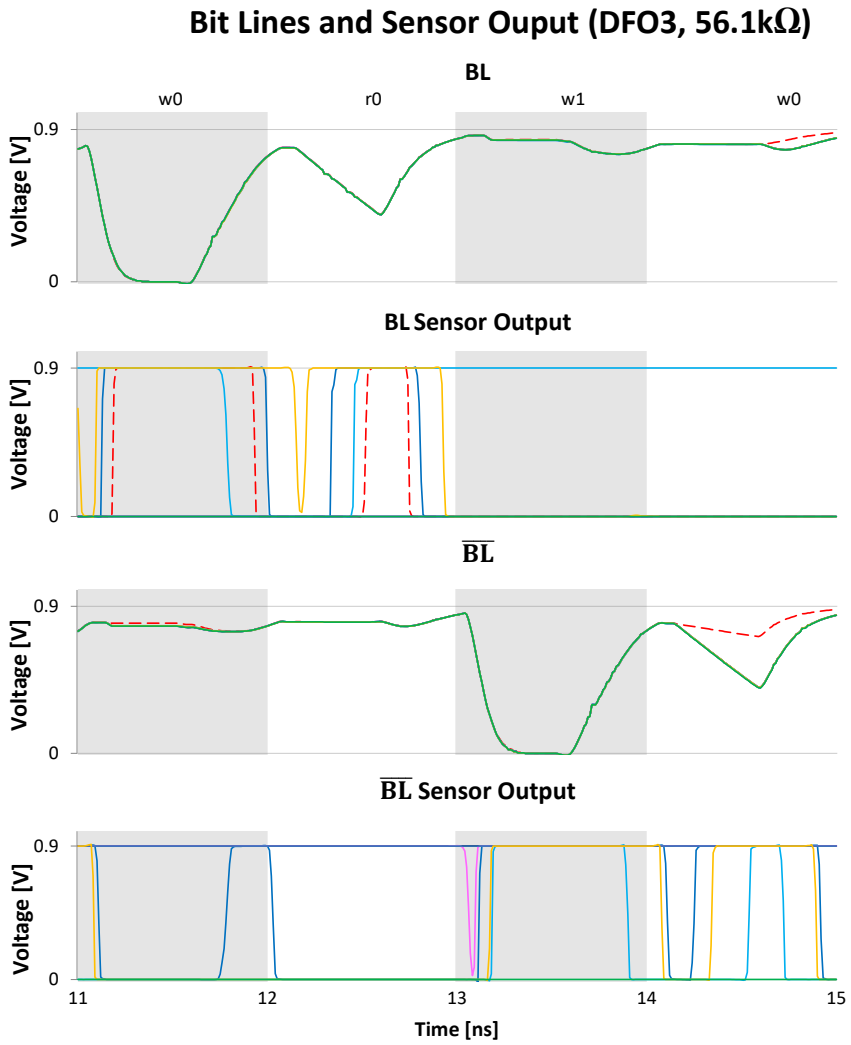


Figure 63: Consumption and Sensor output of an Iteration of the Monte Carlo simulations for the Bitline Voltage Level approach altering only sensors.

5.8.2.3 Discussion

Based on the results presented in the previous sections, it is possible to conclude that both approaches presented deficient behaviors when subjected to intra-die PV. While the current consumption approach demonstrated a certain degree of tolerance when considering only variations in the memory block and peripherals, none of the designed sensors for this work was able to mask the effects of PV on their own structure.

For both approaches, it was also analyzed what is the maximum tolerable degree of variation in parameters. Even with variations smaller than 1%, sensors were not able to differentiate discrepancies caused by resistive defects and discrepancies from the process variation during manufacturing. This strengthens the conclusion that this model of sensor is not tolerant to PV.

As previously stated, designing an analogical circuit for monitoring signals is a complex task. There are many design aspects that contribute and jeopardize the sensor's

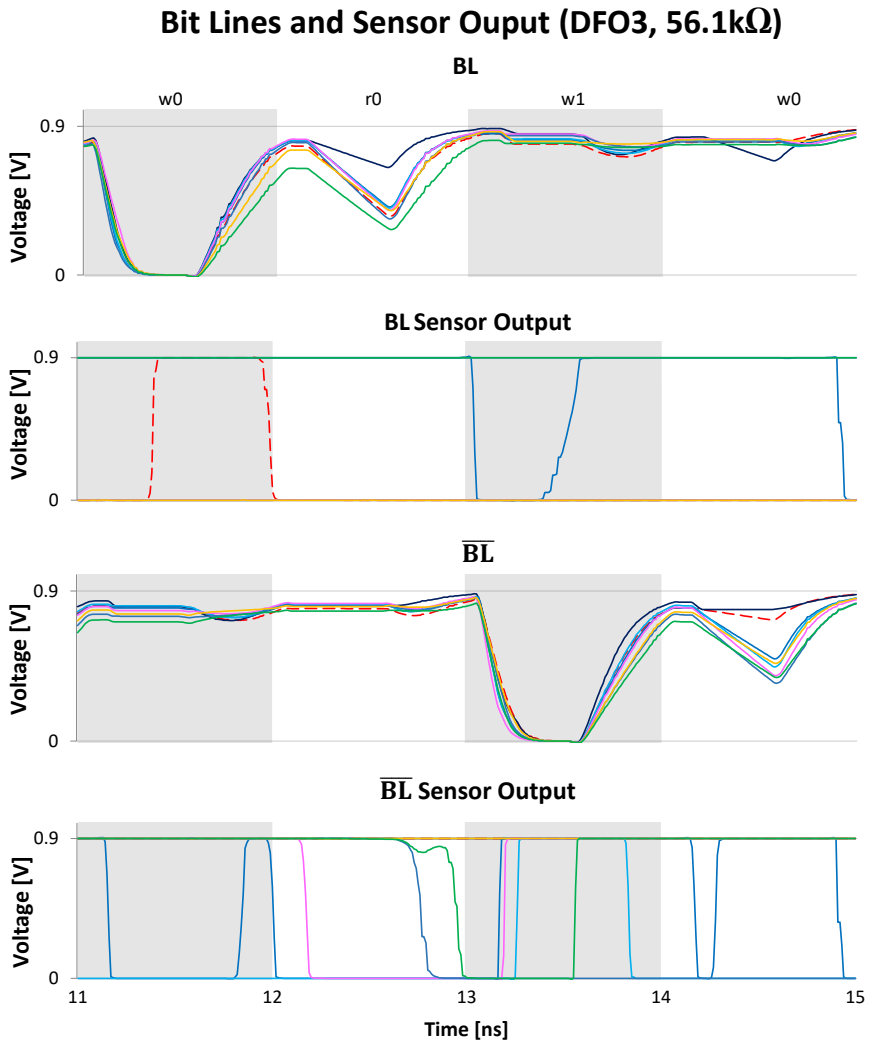


Figure 64: Consumption and Sensor output of an Iteration of the Monte Carlo simulations for the Bitline Voltage Level approach altering all transistor in the circuit.

performance at the same time. In this work, sensors were designed in order that very small discrepancies in the monitored signals were enough for it to generate distinct outputs – and this was achieved, as can be seen in Section 5.4.

However, this also meant that that sensors are very susceptible to not only small variations in the monitored signals, but also variations on their design parameters. A more in-depth analysis is necessary to evaluate the total impact of PV on analogical circuits and therefore on-chip sensors. Only with results from this evaluation will be possible to re-design sensors that are able to produce efficient results and is tolerant to PV.

6 Final Considerations

In this Master's thesis, a hardware-based approach to test FinFET-based SRAMs was presented. The proposed test methodology aimed to identify and detect discrepancies in different aspects of the operation of the memory array produced by resistive defects.

A memory array designed using low-power, 20nm FinFET model by PTM was adopted to perform all simulations in this work. First, a characterization of this model and the memory array built with it was presented. Operations, peripherals, power consumption, and cell's static noise margin were discussed. Then, the set of twelve resistive defects (consisting of 6 resistive-open defects and 6 resistive-bridge defects) were introduced.

With resistive defects defined, the hardware-based approach to detect them was presented. A specification accentuating functional and qualitative requirements was formulated. Implementation divided the methodology in two approaches: one aimed to monitor current consumption, while the other aimed to monitor voltage level on bit lines.

Validations and evaluations were performed for both approaches. Initially, a fault mapping was performed in order to identify critical resistances and faults observed for each resistive defect. Validation of the designed sensors was performed using a March Test that executed 5 operations in each row of the array.

During evaluations, different scenarios of operation were considered to analyze aspects of sensors and memory block as well. Overall, it was evaluated the impact of the sensor on faulty behavior, defect/fault detection capabilities using outputs from sensors, and the impact of temperature on dynamic faults, faulty behavior, and sensor's output. At the end, a brief evaluation of the impact of PV on sensors was carried out.

In general, the sensors proposed in this work presented sufficient results. In nominal temperature of operation, both approaches were able to output distinct signals for very small defects, as it was defined in the specification. When considering a wide range of temperatures of operation, the proposed methodology demonstrated key aspects and limitations for each approach but nevertheless presented acceptable results up to a certain degree.

It is possible to summarize and compare the results obtained during the evaluation of main aspects of the two strategies presented in this work. Regarding the impact on Faulty Behavior, which was presented in Table 4, the bit lines voltage level approach does not have a significant impact on critical resistance, unlike the current consumption approach.

Defect Level	Detection Rate	
	CC	BL
1	71.21%	81.06%
2	81.06%	85.61%
3	86.36%	87.12%
4	85.61%	87.12%
5	86.36%	88.64%
6	87.88%	88.64%
7	87.88%	88.64%
8	87.88%	88.64%
9	87.12%	92.42%
10	88.64%	94.70%

Table 22: Summary of detection rate when altering defect size in temperatures of operation ranging from -40°C to 125°C.

Regarding the sensor's output under nominal temperature, which results were presented in Table 5, it is possible to conclude that even though both approaches presented fair results, first detection of DFB5 on the CC approach happened too close to the critical resistance, thus making the BL approach more efficient.

The results of the evaluation of sensor's output under a wide range of temperature, which was performed by altering temperature of operation from -40°C to 125°C, were presented on Section 5.5, and are summarized on Table 22. If abstracting specific aspects of each approach, the BL approach presented better detection rates.

Area and power were discussed on Subsection 5.7.2 and Subsection 5.7.1, where aspects of overhead were analyzed. Considering the results presented in these Subsections, it is possible to conclude that the BL approach presented better results both in area and power consumption.

Finally, when analyzing the impact of PV on the proposed hardware-based methodology, it became clear that both sensors are very susceptible to intra-die PV. Even though the CC approach presented a better response to variations on the array, all sensors presented a strong susceptibility from PV when their parameters altered. Thus, it is possible to conclude that PV within sensors is the main drawback of this approach.

6.1 Future Work

For future works, it would be desired to thoroughly explore sensor's capabilities to mask the effects of PV on the memory array and within sensors by re-designing them. This could be achieved by a better dimensioning of the sensor and its circuits (such as the PWM generator) or by aggregating new circuits that are able to alleviate the

discrepancies caused by PV. Also, a deeper analysis on the impact of process variation on the designed sensors could be carried out by evaluating how each module (current generator, operational amplifier, converter, PWM, etc.) behaves when subjected to PV. This would provide a better understanding on the characteristics of the adopted sensor model, and further allow a PV-aware design of sensors.

Regarding to the FinFET memories and resistive defects, other works could use the observations reported in this work such as critical resistances and dynamic faults behaviors to analyze the impact of other reliability issues such as Bias Temperature Instability and Single Event Upsets in memory arrays affected by resistive defects. For this dissertation, it was proposed that the sensor should be able to generate distinct outputs for as weak defects as possible. However, up to this point, it is not know how much of a concern these weak defects actually are. Thus, detection of these defects may not compensate for the cost in area invested for it.

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Annex

ANNEX A – Published Works

COPETTI, T. et al. **Gate-level modelling of NBTI-induced delays under process variations**. 2016 17th Latin-American Test Symposium (LATS). **Anais**...IEEE, 2016

COPETTI, T. et al. NBTI-Aware Design of Integrated Circuits: A Hardware-Based Approach for Increasing Circuits' Life Time. **Journal of Electronic Testing**, v. 32, n. 3, p. 315–328, 16 jun. 2016.

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JENIHHIN, M. et al. Identification and Rejuvenation of NBTI-Critical Logic Paths in Nanoscale Circuits. **Journal of Electronic Testing**, v. 32, n. 3, p. 273–289, 12 jun. 2016

MARTINS, M. T. et al. **Analyzing NBTI impact on SRAMs with resistive-open defects**. 2016 17th Latin-American Test Symposium (LATS). **Anais**...IEEE, 2016

MEDEIROS, G. C.; POEHLS, L. B.; VARGAS, F. F. **Analyzing the Impact of SEUs on SRAMs with Resistive-Bridge Defects**. 2016 29th International Conference on VLSI Design and 2016 15th International Conference on Embedded Systems (VLSID). **Anais**...IEEE, jan. 2016

ANNEX B – Automated Tool's Report

```
==========================================================
        Automatic Fault Detector
        Guilherme Cardoso Medeiros
        Version: Thiago
        Defect on analysis: rodf_3
        Generated on  2017-4-24 16:27:30
==========================================================

----------------------------------------------------------
Mode: Transition Analysis
Waveform: 1_W0
No Fault found!!
-----------------------------------
Mode: Transition Analysis
Waveform: 0_W1
No Fault found!!
----------------------------------------------------------
----------------------------------------------------------
Mode: Static Read Destructive Fault Analysis, Cell Bit Read
Waveform: 1_W0R0
No Fault found!!
-----------------------------------
Mode: Static Read Destructive Fault Analysis, Cell Bit Read
Waveform: 0_W0R0
No Fault found!!
-----------------------------------
Mode: Static Read Destructive Fault Analysis, Cell Bit Read
Waveform: 1_W1R1
Lower Limit: 8400        Step: 400
-----------------------------------
Mode: Static Read Destructive Fault Analysis, Cell Bit Read
Waveform: 0_W1R1
Lower Limit: 8400        Step: 400
----------------------------------------------------------
----------------------------------------------------------
Mode: Dynamic Read Destructive Fault Analysis, Cell Bit Read
Waveform: 1_W0R0x50
No Fault found!!
-----------------------------------
Mode: Dynamic Read Destructive Fault Analysis, Cell Bit Read
Waveform: 0_W0R0x50
No Fault found!!
-----------------------------------
Mode: Dynamic Read Destructive Fault Analysis, Cell Bit Read
Waveform: 1_W1R1x50
Lower Limit: 7800        Step: 200
-----------------------------------
Mode: Dynamic Read Destructive Fault Analysis, Cell Bit Read
Waveform: 0_W1R1x50
Lower Limit: 7800        Step: 200
```

```
-------------------------------------------------------------------------
-------------------------------------------------------------------------
Mode: Static Incorrect Read Fault Analysis, Output Read
Waveform: 1_W0R0
No Fault found!!
-------------------------------------
Mode: Static Incorrect Read Fault Analysis, Output Read
Waveform: 0_W0R0
No Fault found!!
-------------------------------------
Mode: Static Incorrect Read Fault Analysis, Output Read
Waveform: 1_W1R1
Lower Limit: 8400          Step: 400
-------------------------------------
Mode: Static Incorrect Read Fault Analysis, Output Read
Waveform: 0_W1R1
Lower Limit: 8400          Step: 400
-------------------------------------------------------------------------
-------------------------------------------------------------------------
Mode: Dynamic Incorrect Read Fault Analysis, Output Read
Waveform: 1_W0R0x50
No Fault found!!
-------------------------------------
Mode: Dynamic Incorrect Read Fault Analysis, Output Read
Waveform: 0_W0R0x50
No Fault found!!
-------------------------------------
Mode: Dynamic Incorrect Read Fault Analysis, Output Read
Waveform: 1_W1R1x50
Lower Limit: 7800          Step: 200
-------------------------------------
Mode: Dynamic Incorrect Read Fault Analysis, Output Read
Waveform: 0_W1R1x50
Lower Limit: 7800          Step: 200
-------------------------------------------------------------------------
```

ANNEX C – Detection Tool's Report

Sensor Detection
Guilherme Cardoso Medeiros
Defect on analysis: rodf_4
Generated on 2017-5-24 17:14:15

Res	Det.0	Det.1	Det.2	Det.3	Det.4	Det.5	Det.6	Det.7
3333	O	O	O	O	O	O	O	O
6666	X	O	O	O	O	O	O	O
9999	X	O	O	O	O	O	O	O
13332	X	O	O	O	O	O	O	O
16665	X	O	O	O	O	O	O	O
19998	X	O	O	O	O	O	O	O
23331	X	O	O	O	O	O	O	O
26664	X	O	O	O	O	O	O	O
29997	X	O	O	O	O	O	O	O
33330	X	O	O	O	O	O	O	O
39996	X	O	O	O	O	O	O	O
43329	X	O	O	O	O	O	O	O
49995	X	O	O	O	O	O	O	O
53328	X	O	O	O	O	O	O	O
56661	X	O	O	O	O	O	O	O
59994	X	O	O	O	O	O	O	O
63327	X	O	O	O	O	O	O	O
66660	X	O	O	O	O	O	O	O
69993	X	O	O	O	O	O	O	O
73326	X	O	O	O	O	O	O	O
76659	X	O	O	O	O	O	O	O
79992	X	O	O	O	O	O	O	O
83325	X	O	O	O	O	O	O	O
86658	X	O	O	O	O	O	O	O
89991	X	O	O	O	O	O	O	O
93324	X	O	O	O	O	O	O	O
96657	X	O	O	O	O	O	O	O
99990	X	O	O	O	O	O	O	O

ANNEX D – Detailed Reports

D.1 Impact of Temperature on CC Sensors

	Resistance [kΩ]									
Defect	**Level 1**	**Level 2**	**Level 3**	**Level 4**	**Level 5**	**Level 6**	**Level 7**	**Level 8**	**Level 9**	**Level 10**
DFO1	3.22	6.44	9.66	12.88	16.10	19.32	22.54	25.76	28.98	32.20
DFO2	12.55	25.10	37.65	50.20	62.75	75.30	87.85	100.40	112.95	125.50
DFO3	6.42	12.84	19.26	25.68	32.10	38.52	44.94	51.36	57.78	64.20
DFO4	5.00	10.00	15.00	20.00	25.00	30.00	35.00	40.00	45.00	50.00
DFO5	212.00	424.00	636.00	848.00	1060.00	1272.00	1484.00	1696.00	1908.00	2120.00
DFO6	279.00	558.00	837.00	1116.00	1395.00	1674.00	1953.00	2232.00	2511.00	2790.00
DFB1	72.01	68.22	64.43	60.64	56.85	53.06	49.27	45.48	41.69	37.90
DFB2	42.94	40.68	38.42	36.16	33.90	31.64	29.38	27.12	24.86	22.60
DFB3	141.17	133.74	126.31	118.88	111.45	104.02	96.59	89.16	81.73	74.30
DFB4	34.01	32.22	30.43	28.64	26.85	25.06	23.27	21.48	19.69	17.90
DFB5	53.01	50.22	47.43	44.64	41.85	39.06	36.27	33.48	30.69	27.90
DFB6	42.56	40.32	38.08	35.84	33.60	31.36	29.12	26.88	24.64	22.40

Table 23: Resistance assigned to each level for each defect for the Current Consumption Approach.

	Temperature										
Defect	-40ºC	-23.5ºC	-7ºC	9.5ºC	27ºC	42.5ºC	59ºC	75.5ºC	92ºC	108.5ºC	125ºC
DFO1	30%	30%	90%	100%	90%	90%	90%	80%	80%	80%	80%
DFO2	0%	100%	100%	100%	100%	100%	100%	90%	90%	90%	90%
DFO3	10%	80%	100%	100%	100%	100%	100%	90%	90%	90%	90%
DFO4	20%	30%	90%	70%	100%	100%	90%	90%	80%	80%	90%
DFO5	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
DFO6	0%	20%	100%	100%	100%	100%	100%	100%	100%	100%	100%
DFB1	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
DFB2	0%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
DFB3	0%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
DFB4	0%	90%	100%	100%	100%	100%	100%	100%	100%	100%	100%
DFB5	10%	60%	100%	100%	80%	70%	100%	0%	0%	0%	0%
DFB6	0%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%

Table 24: Discrepancy detection rate for each of the resistive defects for the Current Consumption approach.

	Temperature										
Level	-40ºC	-23.5ºC	-7ºC	9.5ºC	27ºC	42.5ºC	59ºC	75.5ºC	92ºC	108.5ºC	125ºC
Level 1	33%	50%	83%	83%	83%	83%	67%	33%	33%	33%	33%
Level 2	50%	50%	100%	83%	100%	100%	100%	83%	67%	67%	83%
Level 3	33%	67%	100%	100%	100%	100%	100%	100%	100%	100%	100%
Level 4	17%	50%	100%	83%	100%	100%	100%	100%	100%	100%	100%
Level 5	33%	50%	83%	100%	100%	100%	100%	100%	100%	100%	100%
Level 6	17%	83%	100%	100%	100%	100%	100%	100%	100%	100%	100%
Level 7	33%	50%	100%	100%	100%	100%	100%	100%	100%	100%	100%
Level 8	17%	67%	100%	100%	100%	100%	100%	100%	100%	100%	100%
Level 9	17%	50%	100%	100%	100%	100%	100%	100%	100%	100%	100%
Level 10	17%	83%	100%	100%	100%	100%	100%	100%	100%	100%	100%

Table 25: Discrepancy detection rate for resistive-open defects for the Current Consumption approach.

	Temperature										
Level	-40ºC	-23.5ºC	-7ºC	9.5ºC	27ºC	42.5ºC	59ºC	75.5ºC	92ºC	108.5ºC	125ºC
Level 1	33%	100%	100%	100%	100%	83%	100%	83%	83%	83%	83%
Level 2	17%	83%	100%	100%	83%	83%	100%	83%	83%	83%	83%
Level 3	17%	83%	100%	100%	83%	83%	100%	83%	83%	83%	83%
Level 4	17%	83%	100%	100%	100%	100%	100%	83%	83%	83%	83%
Level 5	17%	83%	100%	100%	100%	100%	100%	83%	83%	83%	83%
Level 6	17%	83%	100%	100%	100%	100%	100%	83%	83%	83%	83%
Level 7	17%	100%	100%	100%	100%	100%	100%	83%	83%	83%	83%
Level 8	17%	100%	100%	100%	100%	100%	100%	83%	83%	83%	83%
Level 9	17%	100%	100%	100%	100%	100%	100%	83%	83%	83%	83%
Level 10	17%	100%	100%	100%	100%	100%	100%	83%	83%	83%	83%

Table 26: Discrepancy detection rate for resistive-bridge defects for the Current Consumption approach.

	Temperature										
Level	-40ºC	-23.5ºC	-7ºC	9.5ºC	27ºC	42.5ºC	59ºC	75.5ºC	92ºC	108.5ºC	125ºC
Level 1	0%	58%	83%	75%	83%	83%	67%	58%	58%	58%	58%
Level 2	0%	42%	83%	75%	92%	92%	92%	83%	75%	75%	83%
Level 3	0%	50%	92%	83%	92%	92%	92%	92%	92%	92%	92%
Level 4	0%	8%	92%	75%	92%	92%	92%	92%	92%	92%	92%
Level 5	0%	25%	83%	83%	92%	92%	92%	92%	92%	92%	92%
Level 6	0%	50%	83%	100%	92%	92%	92%	92%	92%	92%	92%
Level 7	0%	33%	92%	92%	92%	92%	92%	92%	92%	92%	92%
Level 8	0%	17%	100%	100%	100%	100%	92%	92%	92%	92%	92%
Level 9	0%	25%	100%	83%	92%	100%	92%	92%	92%	92%	92%
Level 10	0%	33%	100%	100%	100%	100%	92%	92%	92%	92%	92%

Table 27: Discrepancy detection rate on the V_{DD} sensor for the Current Consumption approach.

	Temperature										
Level	-40ºC	-23.5ºC	-7ºC	9.5ºC	27ºC	42.5ºC	59ºC	75.5ºC	92ºC	108.5ºC	125ºC
Level 1	33%	50%	83%	83%	67%	58%	67%	17%	0%	0%	0%
Level 2	33%	58%	92%	92%	75%	67%	83%	17%	0%	0%	0%
Level 3	25%	58%	92%	100%	75%	75%	83%	17%	0%	0%	0%
Level 4	17%	58%	92%	92%	83%	83%	83%	17%	0%	0%	0%
Level 5	25%	67%	92%	100%	83%	83%	75%	17%	0%	0%	0%
Level 6	17%	58%	100%	100%	83%	83%	83%	17%	0%	0%	0%
Level 7	25%	75%	100%	100%	83%	83%	83%	17%	0%	0%	0%
Level 8	17%	75%	92%	100%	92%	83%	83%	17%	8%	0%	0%
Level 9	17%	75%	100%	100%	92%	83%	83%	17%	8%	0%	0%
Level 10	17%	83%	100%	100%	92%	83%	75%	17%	8%	0%	0%

Table 28: Discrepancy detection rate on the GND sensor for the Current Consumption approach.

D.2 Impact of Temperature on BL Sensors

	Resistance [kΩ]									
Defect	**Level 1**	**Level 2**	**Level 3**	**Level 4**	**Level 5**	**Level 6**	**Level 7**	**Level 8**	**Level 9**	**Level 10**
DFO1	1.50	3.00	4.50	6.00	7.50	9.00	10.50	12.00	13.50	15.00
DFO2	16.10	32.20	48.30	64.40	80.50	96.60	112.70	128.80	144.90	161.00
DFO3	8.00	16.00	24.00	32.00	40.00	48.00	56.00	64.00	72.00	80.00
DFO4	5.00	10.00	15.00	20.00	25.00	30.00	35.00	40.00	45.00	50.00
DFO5	165.00	330.00	495.00	660.00	825.00	990.00	1155.00	1320.00	1485.00	1650.00
DFO6	252.00	504.00	756.00	1008.00	1260.00	1512.00	1764.00	2016.00	2268.00	2520.00
DFB1	71.44	67.68	63.92	60.16	56.40	52.64	48.88	45.12	41.36	37.60
DFB2	25.84	24.48	23.12	21.76	20.40	19.04	17.68	16.32	14.96	13.60
DFB3	85.12	80.64	76.16	71.68	67.20	62.72	58.24	53.76	49.28	44.80
DFB4	25.84	24.48	23.12	21.76	20.40	19.04	17.68	16.32	14.96	13.60
DFB5	49.40	46.80	44.20	41.60	39.00	36.40	33.80	31.20	28.60	26.00
DFB6	39.14	37.08	35.02	32.96	30.90	28.84	26.78	24.72	22.66	20.60

Table 29: Resistance assigned to each level for each defect for the Bit Line Voltage Level Approach.

	Temperature										
Level	-40ºC	-23.5ºC	-7ºC	9.5ºC	27ºC	42.5ºC	59ºC	75.5ºC	92ºC	108.5ºC	125ºC
Level 1	100%	50%	100%	100%	83%	67%	50%	50%	50%	50%	50%
Level 2	100%	67%	100%	100%	100%	67%	50%	67%	67%	67%	67%
Level 3	100%	67%	100%	100%	100%	67%	67%	67%	67%	67%	83%
Level 4	100%	67%	100%	100%	100%	67%	67%	67%	67%	67%	83%
Level 5	100%	67%	100%	100%	100%	83%	67%	67%	67%	83%	83%
Level 6	100%	67%	100%	100%	100%	83%	67%	67%	67%	83%	83%
Level 7	100%	67%	100%	100%	100%	83%	67%	67%	67%	83%	83%
Level 8	100%	67%	100%	100%	100%	83%	67%	67%	67%	83%	83%
Level 9	100%	67%	100%	100%	100%	83%	83%	83%	83%	83%	83%
Level 10	100%	83%	100%	100%	100%	100%	83%	83%	83%	83%	83%

Table 30: Discrepancy detection rate for resistive-open defects for the Bit Line Voltage Level approach.

	Temperature										
Level	-40ºC	-23.5ºC	-7ºC	9.5ºC	27ºC	42.5ºC	59ºC	75.5ºC	92ºC	108.5ºC	125ºC
Level 1	100%	83%	100%	100%	100%	100%	83%	83%	83%	100%	100%
Level 2	100%	83%	100%	100%	100%	100%	83%	83%	83%	100%	100%
Level 3	100%	83%	100%	100%	100%	100%	83%	83%	83%	100%	100%
Level 4	100%	83%	100%	100%	100%	100%	83%	83%	83%	100%	100%
Level 5	100%	83%	100%	100%	100%	100%	83%	83%	83%	100%	100%
Level 6	100%	83%	100%	100%	100%	100%	83%	83%	83%	100%	100%
Level 7	100%	83%	100%	100%	100%	100%	83%	83%	83%	100%	100%
Level 8	100%	83%	100%	100%	100%	100%	83%	83%	83%	100%	100%
Level 9	100%	100%	100%	100%	100%	100%	83%	83%	100%	100%	100%
Level 10	100%	100%	100%	100%	100%	100%	83%	100%	100%	100%	100%

Table 31: Discrepancy detection rate for resistive-bridge defects for the Bit Line Voltage Level approach.